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(54) Data transmission apparatus.

(57) An ADRC encoder generates, regarding an ADRC block of 4x4 pixels, DR, MIN and quantized data corresponding to each pixel. A macro block formatting circuit generates code data DR, MIN and DT of four ADRC blocks. An adding circuit generates sum data (DR =DR1 + DR2 + DR3 + DR4, same calculation regarding MIN) of important data in the macro block. Mixing circuits insert the sum data into recording data as additional data. The sum data and the important data are distributed and recorded in plural channels. If one of the important data has an error and the remaining important data and the sum data have no error, the important data with the error can be completely corrected. Error correction of the important data and the quantized data generated by block encoding is effected with restrained increase in redundancy. Input data which has been reproduced and DCT-decoded is supplied to and is converted into 3x3 block format by a 3-line memory and block formatting circuit . An ADRC encoding circuit generates encoded data DTx of a center pixel data and data DT which is made up of peripheral 8 pixel data. A timing aligning circuit generates class information comprising 8 pixel data and the class information is supplied to a memory as a read address. Memory stores existing-range data and predicted data DTx' through in-advance training. An error is detected by comparing the existing-range data and reproduced data DTx and when there is an error, predicted data DTx is selected. Error correction of received or reproduced image data is effected without using an error correction code.

FIG. 5(A)

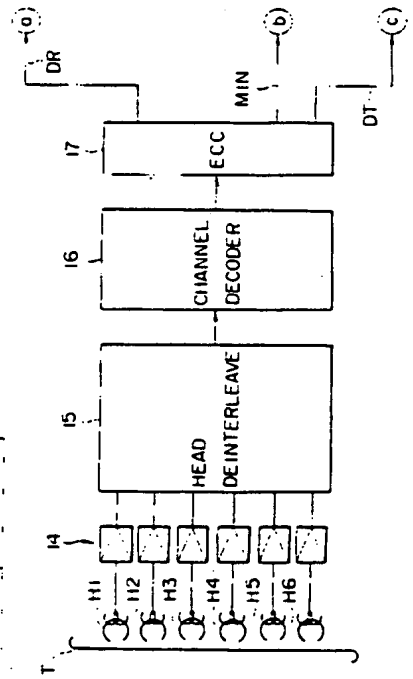

FIG 5 | FIG.5(A) | FIG.5(B)

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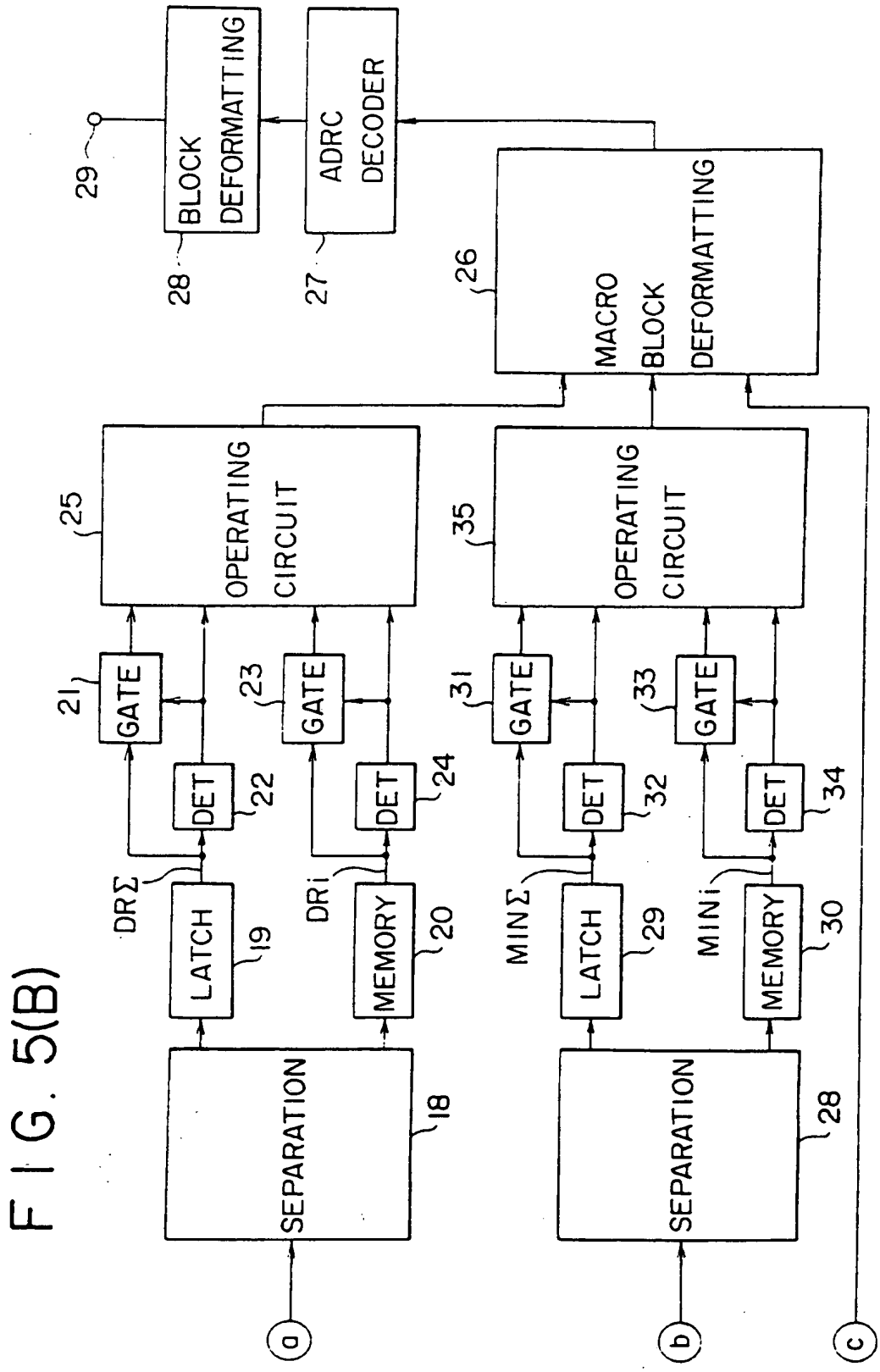


FIG. 5(B)

This invention relates to data transmission apparatus for transmitting (including recording and/or reproducing) code data, and is applicable for example to a digital video tape recorder (VTR) where digital video signals are encoded by block encoding to compress the amount of data so that the digital video signals are divided into small blocks and are processed block by block.

When digital video signals are recorded on a recording medium such as a magnetic tape, it is conventional to compress the digital video signals by high-efficiency encoding in order to make the transmission rate low enough to record/reproduce, because the data amount of the digital video signals is large. Block encoding, such as ADRC (Adaptive Dynamic Range Coding) and DCT (Discrete Cosine Transform), which divide digital video signals into small blocks and encodes them block by block, are known as high-efficiency encoding techniques.

ADRC is a high-efficient encoding which calculates a dynamic range defined by maximum and minimum levels of pixel data among plural pixels included in a two-dimensional block, and encodes the pixel data in accordance with the dynamic range, as described in Japanese Laid-open patent 61-144989. DCT is to cosine-transform pixels in a block, to re-quantize co-efficient data obtained by the cosine-transformation, and to encode them by variable-length encoding. Another encoding method has been suggested in which data averages of every blocks and the difference between each pixel data and the average in each block are vector-quantized.

Code outputs resulting from a block encoding do not have equal importance. In ADRC, if dynamic range information is unknown at the reproducing side, errors extend to all pixels of that block. Therefore, the dynamic range information which is obtained for every blocks is more important than the code signal which is obtained for every pixels. In one type of ADRC in which the number of bits for quantization varies depending upon the dynamic range, if there is an error about the dynamic range, the number of bits for quantization of that block cannot be identified at the receiving side. As a result, the boundaries between that block and other blocks become unknown so that errors extend to the other blocks. Among coefficient data generated in DCT encoding, a DC (direct current) component is more important than AC (alternating current) components. A refresh data in DPCM encoding is also important data.

When outputs of block encoding are recorded/reproduced by a digital VTR, for example, an error correction code is used to protect data against recording/reproducing errors. When an important data happens to have an error which the error correction code cannot correct, the error extends to the whole block. To cure the problem, the same important data is recorded twice at locations separate enough to be not subject to a burst error. However, redundancy would increase and efficiency of data compression would be lowered.

With respect to a block having an error in important data, the error of the important data is statistically presumed based upon spacial correlation between that block and peripheral blocks. In the more concrete, A least-squares method using the code data of the error block and the decoded data located at boundaries of the peripheral blocks may be also used to presume the important data in the error block. The maximum and minimum values of boundary data of the peripheral blocks may be used to presume the important data. The presumed important data is used for decoding. Even though the important data is presumed with high accuracy, original important data cannot be restored completely. In addition, finding boundaries between each data block correctly is necessary to presume the important data. Therefore, if an error extends to several blocks, the important data cannot be presumed.

When digital video signals are recorded/reproduced in a digital VTR for example, it is also conventional to use error correction coding for correcting errors. As an error correction code, simple parity, Read-Solomon code and a combination of these and interleaving have been practically used.

However, when an error correction code is used, redundancy of data increases due to an increase in the number of parity bits in order to improve an error correction ability. When the error cannot be corrected by the error correction code, a conceal circuit would be necessary to interpolate pixel having an error with peripheral correct pixel data. Data such as a computer software generally has no correlation. However, video signals have a correlation in space and in time.

Preferred embodiments of the invention described below provide: a data transmission apparatus for transmitting (including recording and/or reproducing) block code data, which can correct errors of important data or quantized data, with restrained increase of redundancy; a data transmission apparatus for transmitting (including recording and/or reproducing) digital video signals without using an error correction code, taking advantage of spacial correlation of the video signals; and a data transmission apparatus for transmitting digital data having a correlation such as video signals and for correcting data having errors without using an error correction code.

There is provided, in accordance with one aspect of the present invention, a data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein the block code data includes important data which has high importance for decoding purpose, the *trans-*

mission apparatus being characterized in that: a sum data of the plural important data is formed; the sum data is transmitted in time and space different from that of the plural important data; and the plural important data are restored from the received sum data and the received plural important data.

In another aspect of the present invention, there is provided a data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein the block code data includes important data which has high importance for decoding purpose and wherein the block code data is transmitted in plural channels, the transmission apparatus being characterized in that: a sum data is formed by operating the fewer number of the important data than the number of the channels; the sum data is transmitted in a channel other than channels constituting the sum data; and the plural important data are restored from the received sum data and the received plural important data.

In another aspect of the present invention, there is provided a data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein the block code data includes important data which has high importance for decoding purpose, the transmission apparatus being characterized in that: a weighted average data is formed for the plural important data; the weighted average data is transmitted in time and space different from that of the plural important data; and the plural important data are restored from the received weighted average data and the received plural important data.

In another aspect of the present invention, there is provided a data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein the block code data includes important data which has high importance for decoding purpose, the transmission apparatus being characterized in that: a sum data is formed for a unit of the plural important data by operating the plural important data in that unit and at least one important data in another unit; the sum data is transmitted in time and space different from that of the plural important data; and the plural important data are restored from the received sum data and the received plural important data.

In another aspect of the present invention, there is provided a data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein the block code data includes important data which has high importance for decoding purpose, the transmission apparatus being characterized in that: a sum data is formed for a unit of the plural important data by operating the plural important data in that unit and at least one important data in another unit, wherein a type of the plural important data changes regularly; the sum data is transmitted in time and space different from that of the plural important data; and the plural important data are restored from the received sum data and the received plural important data.

In another aspect of the present invention, there is provided a data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein the block code data includes plural data, the transmission apparatus being characterized in that: a sum data of the plural data is formed; the sum data is transmitted in time and space different from that of the plural data; when one of the received plural data has an error, the data having an error is restored from the sum data and the remaining plural data having no error; when a plurality of the received data have errors, an interpolated data is formed by interpolating the data having an error in space or in time; and the errors of the received plural data are corrected based upon the interpolated data and the sum data.

In another aspect of the present invention, there is provided a data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein the block code data includes plural data, the transmission apparatus being characterized in that: a sum data is formed by adding bit data from MSB to a predetermined bit position with respect to the plural data; the sum data is transmitted in time and space different from that of the plural data; and the plural data are restored from the received sum data and the received plural data.

As described above, important data in ADRC are dynamic range DR and minimum value MIN. The sum data of n dynamic range data DR and the sum data of n minimum data MIN are inserted into transmitted data. If one of DRs and MINs has an error and the sum data and the other important data have no error, the correct important data can be reproduced at the receiving side. Redundancy can be lower than when the same important data is recorded several times.

A data transmission apparatus for transmitting digital video signals according to further aspect of the present invention, comprises an error detecting circuit for detecting errors of received or reproduced digital video signals, wherein the error detecting circuit comprises a clustering circuit for clustering based

upon plural pixel signals proximate in space or in time to a pixel to be detected, a memory circuit for storing existing-range data which has been provided in advance by training for each class, a reading circuit for reading out the existing-range data for an class corresponding to an address data which is defined by the output of the clustering circuit, and a comparing circuit for comparing the output of the reading circuit and the pixel data of the pixel to be detected, whereby whether an error exist or not is detected based upon the output of the comparing circuit.

In another aspect of the present invention, there is provided the above data transmission apparatus for transmitting digital video signals, wherein the memory circuit further stores information regarding representative data for each class, and wherein the pixel data to be detected is substituted with representative data formed based upon the information regarding representative data when the existence of an error is detected based upon the output of the comparing circuit.

In another aspect of the present invention, there is provided the above data transmission apparatus for transmitting digital video signals, wherein the reproduced or received digital video signals are encoded video signals, the apparatus further comprises a decoding circuit for decoding the encoded video signals, and the clustering circuit clusters based upon the decoded outputs of plural pixel data proximate to the pixel data to be detected.

In another aspect of the present invention, there is provided the above data transmission apparatus for transmitting digital video signals, wherein the encoded video signals are made by variable-length encoding of coefficient data obtained by DCT.

In another aspect of the present invention, there is provided the above data transmission apparatus for transmitting digital video signals, wherein the clustering circuit comprises an ADRC encoding circuit and is supplied with the pixel data to be detected and the plural pixel data proximate thereto, and among the encoded data the encoded data corresponding to the plural pixel data are used as a class information.

In another aspect of the present invention, there is provided the above data transmission apparatus for transmitting digital video signals, wherein the existing-range defining data is the maximum and minimum of actual data detected for each class.

In another aspect of the present invention, there is provided the above data transmission apparatus for transmitting digital video signals, wherein the information regarding representative data is an average of the actual data detected for each class.

In another aspect of the present invention, there is provided the above data transmission apparatus for transmitting digital video signals, wherein the existing-range defining data is coefficient data which is operated with the plural proximate pixel data, and an error allowance information.

In another aspect of the present invention, there is provided the above data transmission apparatus for transmitting digital video signals, wherein the information regarding representative data is coefficient data which is operated with the plural proximate pixel data and wherein the representative data results from the operation of the coefficient data and the plural proximate pixel data.

In another aspect of the present invention, there is provided the above data transmission apparatus for transmitting digital video signals, wherein the apparatus further comprises a counter circuit for counting the number of pixels having detected errors in a certain period and wherein the error allowance information can vary in accordance with the output of the counter circuit.

As described above, by clustering based upon a pixel to be detected and its peripheral data and by comparing signal level range of the current pixel provided for each class with the actual level, an error is detected based upon its probability and the pixel having the detected error is corrected by substituting it with a predicted data which had been provided for each class.

The invention will now be further described, by way of illustrative and non-limiting example, with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of an example of a recording circuit for a digital VTR to which the present invention can apply.

Fig. 2 shows an example of a recording pattern in an embodiment of the present invention.

Fig. 3 shows an example of a construction of a ADRC block in an embodiment of the present invention.

Fig. 4 shows an example of a construction of a macro block in an embodiment of the present invention.

Fig. 5 is a block diagram of an example of a reproducing circuit for a digital VTR to which the present invention can apply.

Fig. 6 is a block diagram of an example of a sum data generating circuit in an embodiment of the present invention.

Fig. 7 is a timing chart for explanation of a sum data generating circuit in an embodiment of the present invention.

Fig. 8 is a block diagram of another example of a mixed sum data generating circuit.

Fig. 9 is a timing chart for explanation of another example of a mixed sum generating circuit.

Fig . 10 is a block diagram of further example of a mixed sum generating circuit.

Fig. 11 is for explanation of further example of a mixed sum generating circuit.

Fig. 12 is a timing chart for explanation of further example of a mixed sum generating circuit.

Fig. 13 is a block diagram of still further example of a mixed sum generating circuit.

Fig. 14 is a timing chart for explanation of still further example of a mixed sum generating circuit.

Fig. 15 is a drawing for explanation of a mixed sum generating circuit which applies to quantized data.

Fig. 16 is an overall block diagram of a recording/reproducing circuit for a digital VTR to which the present invention can apply.

Fig. 17 is a block diagram of an example of a correction circuit according to the present invention.

Fig. 18 is a block diagram of an example of a construction for forming a data for correction.

Fig. 19 is a drawing for explanation of block formatting.

Fig. 20 is a block diagram of an example of 1-bit ADRC encoding circuit.

Fig. 21 is a block diagram of an example of a practical construction for forming a data for correction.

Fig. 22 is a block diagram of another example of a correction circuit according to the present invention.

Fig. 23 is a block diagram of another example of a construction for forming a data for correction.

Fig. 24 is a block diagram of further example of a correction circuit according to the present invention.

Fig. 25 is a drawing for explanation of the further example of a correction circuit according to the present invention.

Fig. 26 is a drawing for explanation of error correction circuit according to the present invention.

An embodiment of the present invention will be described hereinafter. Fig. 1 shows an embodiment, that is, an outline construction of signal processing for a digital VTR. Digital video signals are supplied from an input terminal 1. This input signals have 8-bit data for each pixel, for example. The input digital video signals are supplied to a block-formatting circuit 2. In this embodiment, block-formatting circuit 2 divides a valid area of one frame into blocks each having 4×4 pixels, 8×8 pixels, or something like that.

Block-formatting circuit 2 supplies to an ADRC encoder 3 digital video signals which had been scan-converted in the order of the blocks. ADRC encoder 3 compresses pixel data block by block. ADRC encoder 3 supplies encoded output to a macro-block-making circuit 4. A macro block comprises a plurality of ADRC blocks which have been made by block-formatting circuit 2.

ADRC encoder 3 detects dynamic range DR and minimum value MIN of each block. ADRC encoder 3 re-quantizes the video data less minimum value MIN by a quantizing step. In ADRC using a fixed 4-bit length, quantizing step Δ can be obtained by dividing dynamic range DR by 16. The video data less the minimum value is divided by quantizing step Δ. Integral part of quotient is a quantized data DT. Dynamic range DR, minimum value MIN and quantized data DT are output data of ADRC encoder 3. Each block has dynamic range DR and minimum value MIN as important data.

Macro block-formatting circuit 4 generates coded data of macro blocks. Quantized data DT of the macro blocks are supplied to an error correction encoder 5. Dynamic range DR and minimum value MIN of the macro blocks are supplied to an adding circuit 6. Adding circuit 6 generates the sum data DRΣ of plural dynamic ranges DRs and the sum data MINΣ of plural minimum values MINs included in a macro block.

These sum data are supplied through memories 7 and 8 to mixing circuits 9 and 10. Original important data (DR, MIN), which have been through adding circuit 6, are supplied to mixing circuits 9 and 10. The outputs of mixing circuits 9 and 10 are supplied to error correction encoder 5.

The output data of ADRC encoder 3 is supplied to error correction encoder 5. Error correction encoder 5 generates a parity of an error correction code. A product code can be utilized as an example of the error correction code. In a product code, data are arranged as a matrix and error correction encoding applies to each of horizontal and vertical directions of the matrix. Block synch signal (SYNC) and ID signal are added to the code data and the parity. Record data having continual synch blocks are supplied to a channel encoder 11 which channel-encodes the record data in order to reduce a direct current component.

The output data of channel encoder 11 is supplied to a head interleave circuit 12. Head interleave circuit 12 generates six channels of record data. Head interleave circuit 12 supplies each channel of the record data through a recording amplifier 13 to rotary heads H1-H6. Head interleave circuit 12 interleaves the recording data among the plural channels. Rotary heads H1-H6 simultaneously form six tracks on a magnetic tape T.

Fig. 2 shows a recording pattern formed on magnetic tape T. Respective slant tracks corresponding to respective heads H1 - H6 have respective references CH1 - CH6.

In this embodiment, as shown in Fig. 3, one ADRC block has (4×8) pixels. Assuming that a valid area of one field of video has (240 lines × 720 pixels), (60 × 90) ADRC blocks are formed in one field, as shown in Fig. 4. Further assuming that a macro block has (2×2 = 4) ADRC blocks, adding circuit 6 carries out the following adding calculations to generate the sum data DRΣ and MINΣ.

$$DR\Sigma = DR1 + DR2 + DR3 + DR4$$

$$MIN\Sigma = MIN1 + MIN2 + MIN3 + MIN4$$

When each important data is 8-bit data, 10-bit sum data is generated.

As shown in Fig. 4, head interleave circuit 12 dis-

tributes four important data and their sum data into different channels. For example, when each code data of four ADRC blocks of an upper-left cornered macro block in Fig. 4 is recorded in CH1, CH2, CH3, and CH4, respectively, the sum data DRΣ and MINΣ, which are the sum of the important data of these ADRC blocks, are recorded in the first channel (CH6) of the following macro block (right hand sided macro block).

In this way, the four important data and the sum data of them are recorded in different channels. Therefore, even if the whole data of the first channel cannot be reproduced due to a head clog, for example, the important data of the first channel can be corrected as follows.

$$DR1 = DR\Sigma - DR2 - DR3 - DR4$$

$$MIN1 = MIN\Sigma - MIN2 - MIN3 - MIN4$$

When important data of each block is recorded twice, as in prior art, additional 16 bits are necessary per one ADRC block. On the other hand, according to the present invention, since additional 20 bits are necessary per one macro block, only additional 5 bits are necessary one ADRC block and perfect correction can be achieved.

Referring to Fig. 5, a reproducing circuit which corresponds to the recording circuit as shown in Fig. 1 will be described. Each channel of reproduced data reproduced from magnetic tape T by six rotary heads H1-H6 is supplied through a reproducing amplifier 14 to a head de-interleave circuit 15. Head de-interleave circuit 15 de-interleaves the reproduced data which had been interleaved by head interleave circuit 12 at the recording side.

Head de-interleave circuit 15 supplies its output data to a channel decoder 16 which channel-decodes the supplied data. Channel decoder 16 supplies its output data to an error correction circuit 17 which decodes the product code. The output data of error correction circuit 17 includes, in addition to the reproduced data, an error flag to show whether an error exists after the error correction.

Important data DR and MIN included in the output data of error correction circuit 17 are corrected by the above algorism. Dynamic range DR of a macro block is supplied to a separation circuit 18. Separation circuit 18 separates the sum data DRΣ and DRi. A latch 19 latches the sum data DRΣ and the error flag and a memory 20 stores DRi and the error flag.

Latch 19 supplies the sum data DRΣ through a gate circuit 21 to an operating circuit 25. Latch 19 also supplies the error flag to a detecting circuit 22 whose output is supplied to gate circuit 21 and operating circuit 25. Memory 20 supplies Fri and the error flag to a gate circuit 23 and a detecting circuit 24. Gate circuit 23 is controlled by a detecting signal from detecting circuit 24. Outputs of gate circuit 23 and detecting circuit 24 are supplied to operating circuit 25.

The same circuit construction as the above-explained one for the error correction of dynamic range DR is provided for the error correction of minimum value MIN. Circuit blocks for minimum value MIN will have reference numerals which are made up by adding ten and the reference numerals used for the circuit blocks for dynamic range DR. Explanation thereof will be omitted.

Corrected dynamic range from operating circuit 25, corrected minimum value MIN from operating circuit 35 and code data DT from error correction circuit 17 are supplied to a macro block deformatting circuit 26. Macro block deforming circuit 26 deforms the supplied data into reproduced data of every ADRC block. The reproduced data of each ADRC block are supplied to an ADRC decoder 27 where ADRC decoding process is done.

In ADRC decoding where the bit number of quantized code is 4 bits, decoded data Li is generated for every pixel. Decoded data Li is expressed as follows :

$$Li = [(DR / 2^4) \times xi + MIN + 0.5]$$

$$[\Delta \times xi + MIN + 0.5]$$

Xi is a value of code signal, Δ is a quantizing step and [ ] means a gaussian mark. Calculation inside [ ] mark can be achieved by using a ROM, for example. ADRC decoder 27 has a function of adding minimum value MIN.

ADRC decoder 27 supplies its output to a block deformatting circuit 28. Block deformatting circuit 28 changes back the order of data from a block order to a raster-scan order. The reproduced data is obtained at an output terminal 29 of block deformatting circuit 28. If necessary, output terminal 29 may have an error interpolation circuit. The error interpolation circuit interpolates a pixel data having an error with peripheral pixel data.

Fig. 6 shows one example of gate circuits 21 and 23 and operating circuit 25. DRi is supplied to an input terminal 41. The detect signal from detecting circuit 24 is supplied to an input terminal 42. The sum data DRΣ is supplied to an input terminal 43. The detect output from detecting circuit 22 is supplied to an input terminal 44. Gate circuit 23 supplies DRi to an accumulating circuit 47 and an arrangement control circuit 48. The accumulated output of accumulating circuit 47 and the output of gate circuit 21 are supplied to a subtracting circuit 49. Subtracting circuit 49 supplies its output to arrangement control circuit 48. Corrected important data (dynamic range DR) is derived at an output terminal 50 of arrangement control circuit 48.

As an example case, if DR3 among DR1 - DR4 has an error, as shown in Fig. 7, gate circuit 23 receives the detect signal which becomes high level at the location corresponding to DR3. When a control signal is high level, gate circuit 23 is OFF so that accumulating circuit 47 and arrangement control circuit 48 receive DRi other than DR3. Because it is assumed here that DRΣ has no error, DRΣ will pass

through gate circuit 21.

Accumulating circuit 47 generates an accumulated output (DR1 + DR2 + DR4). Accordingly, subtracting circuit 49 subtracts the accumulated output from DRΣ1 and generates a corrected DR3 at its output. Arrangement control circuit 48 substitutes DR3 in original DRi with the corrected one and generates it. Regarding minimum value MIN, MIN having an error is corrected by operating circuit 35 in the same manner as explained above. The correction is possible when the sum data has no error and only one of plural important data constituting the sum data has an error.

In the above embodiment, one macro block has (2×2) four ADRC blocks. It is possible to change the size of the macro blocks. It is also possible to record the sum data and the plural important data constituting the sum data at separate channels among plural channels so that an error correction ability against a burst error in one channel can be higher. For example, if one macro block comprises sixteen ADRC blocks and six channels of data can be recorded in parallel, sum data of 12-bit is generated as follows:

$$DR\Sigma = DR1 + DR2 + \cdots + DR16$$

$$MINE = MIN1 + MIN2 + \cdots + MIN16$$

DR1 - DR6 and MIN1 - MIN6 are recorded into channels CH1 - CH6, respectively. DR7 - DR12 and MIN7 - MIN12 are recorded into channels CH1 - CH6. DR13 - DR16 are recorded into channels CH1 - CH4 and the sum data is recorded into channel CH5. There is only 1.5 bit increase per ADRC block. In this way, when the size of macro block becomes bigger, important data can be completely corrected with restrained increase of redundancy, when a burst error happens due to a tape damage or like that.

As explained above, when the sum data generated by simple adding is recorded, the bit number increases such as from 8-bit to 10-bit. One of methods to avoid this problem is to record the average (8 bits) of the sum data. When the average is used, an error is generated by rounding. In order to avoid the problem, the sum data of plural important data which had been weighted is averaged to form the average.

When one macro block comprises four ADRC blocks, the sum data is obtained by the following equation. The sum data of minimum values MIN is obtained in the same way.

$$DR\Sigma = (DR1 \times 2 + DR2 \times 1 + DR3 \times 1 + DR4 \times 1) / 5$$

Fig. 8 shows an example of circuits to achieve this calculation. DRi is supplied to an input terminal 51. DRi is then supplied to a circuit 52 for multiplying twice and a circuit 53 (merely having a buffer function). Circuits 52 and 53 supply their outputs to two input terminals of a switching circuit 54. Switching circuit 54 is controlled by a control signal supplied from a terminal 55.

As shown in Fig. 9, switching circuit 54 selects the output of circuit 52 at the timing of DR1 and selects the output of circuit 53 otherwise. Switching circuit 54 supplies its output to an accumulating circuit 56 and the sum data of weighted DRi is derived at an output terminal 57. Although not shown in Fig. 9, a division circuit for dividing by 5 is connected to the output of operating circuit 56.

In forming the average of the weighted sum, an important data which is more important than any other important data would have a bigger weighting factor. In forming four ADRC blocks, for example, if the first ADRC block comprises pixel data in the frame, the second ADRC block comprises the difference data of pixel data between the first and second ADRC blocks and the third and fourth ADRC blocks similarly comprise the difference data, important data DR1 and MIN1 of the first ADRC block comprising pixels having original pixel data are considered more important.

When plural sums data of important data are formed, some of important data constituting the sum data may be used to form both the sum data. Figs. 10 and 11 show such an example. As shown is Fig. 11, let us assume two macro blocks adjacent to each other in the vertical direction. If same reference numeral are put to important data generated from each ADRC block, the sum data are formed as follows :

$$DR\Sigma = DR1 + DR2 + DR3 + DR4 + DR1'$$

$$DR\Sigma' = DR1' + DR2' + DR3' + DR4' + DR1$$

The sum data of minimum values are similarly formed. In this way, when both DR1 and DR2 have errors, they can be corrected if other data have no error. Although DR1 and DR1' are used twice in both equations, DR to be used twice may change regularly.

Referring to Fig. 10, an example of circuit construction for forming the sum data will be described. ADRC decoder supplies its code output to macro block-formatting circuit 4. Dynamic range DR, minimum value MIN and quantized data DT are generated by circuit 4 for every macro block. Dynamic range DR and minimum value MIN are supplied to sum data generating circuits 60a and 60b, respectively.

In mixed sum data generating circuit 60a, as shown in Fig. 11, a timing aligning circuit 65 aligns timings of two macro blocks adjacent to each other in the vertical direction. Timing aligning circuit 65 outputs from one output terminal dynamic range DRs of a macro block comprising ADRC blocks 1-4. Timing aligning circuit 65 outputs from the other output terminal dynamic range DR's of a macro block comprising ADRC blocks 1' - 4'. Timing aligning circuit 65 comprises four line memories.

DRs of one macro block are supplied to an adding circuit 66 and a gate circuit 70. DR's of the other macro block are supplied to an adding circuit 69 and a gate

circuit 67. Through terminals 68 and 71, control signals are supplied to gate circuits 67 and 70 so that only DR1 passes through gate circuit 70, as shown in Fig. 12. Although not shown in figures, the control signal is supplied to gate circuit 67 so that only DR's pass through gate circuit 67.

Accordingly, adding circuit 66 generates a result of addition (DR1 + DR2 + DR3 + DR4 + DR1') and adding circuit 69 generates a result of addition (DR1' + DR2' + DR3' + DR4' + DR1). The output of adding circuit 66 is supplied to a mixing circuit 73 through a delay circuit 72 having a delay of one macro block and is mixed by mixing circuit 73 with an undelayed signal. Similarly, the output of adding circuit 69 is supplied through a delay circuit 74 to a mixing circuit 75 so that mixed sum data is obtained at the timing of the first ADRC block of the next macro block.

The output of mixing circuit 73 is supplied to a rearranging circuit 76 and the output of mixing circuit 75 is supplied through delay circuit 77 to rearranging circuit 76. Delay circuit 77 has a delay of two lines. At an output terminal 62 of rearranging circuit 76, an output data composed of important data and their mixed data is generated.

Regarding minimum value MIN, mixed sum data generating circuit 60b similar to the above-explained is provided. Minimum value MIN and their mixed sum data are derived from an output terminal 63. Quantized code DT is derived from an output terminal 64 after getting through a delay circuit 61 for timing.

By adding plural upper bits of important data to produce sum data, an increase in the number of bits forming the sum data can be restrained without degrading a quality of video. For example, when an macro block has sixteen ADRC blocks, the bit number forming the sum data increases from 8 bits to 12 bits in a case of simple adding. But, if upper 4 bits of sixteen DC components are added, the bit number of the sum data can remain to be 8 bits. If the number of bits selected downward from MSB, accuracy would be lowered, but nearly correct data from can be restored.

Figs. 13 and 14 are used to explain for forming the sum data from upper 4 bits. Fig. 13 shows a construction of circuits for dynamic range DR only. Dynamic range DR from macro block formatting circuit 4 is supplied to a gate circuit 81. Gate circuit 81 is controlled by a control signal supplied from an input terminal 82. The output of gate circuit 81 is supplied to an accumulating circuit 83.

Fig. 14 shows the control signal from input terminal 82 to control gate circuit 81. Serial bits of DR1, DR2, DR3, DR4, ... are supplied to gate circuit 81 and the control signal is at high level during the upper 4 bits periods of DRi. Only during the period of the high level, gate circuit 81 is ON so that accumulating circuit 83 generates the sum data of the upper 4 bits of DRi.

Not only important data, sum data of pixel data may be formed. Fig. 15 shows a construction of (4 × 4) ADRC block. Reference numerals are put on quantized data DT (4 bits) of respective pixels. The sum data is formed according to the following equation:

$$DT\Sigma = DT1 + DT2 + DT3 + \ldots\ldots + DT15 + DT16$$

Sum data DTΣ of these quantized data is also transmitted.

According to this method, DR, MIN, DTΣ and quantized data generated in one ADRC block are transmitted so that one error of quantized data can be corrected. In addition, errors of two quantized data can be interpolated. For example, when DT7' and DT10' have errors, interpolated data is formed by using peripheral pixel data. That is :

$$DT7' = (DT3 + DT6 + DT8 + DT11) / 4$$

$$DT10' = (DT6 + DT9 + DT11 + DT14) / 4$$

(Mark ' means interpolation). Ratio of these interpolated data is calculated and the sum data DTΣ is apportioned according to the ratio. In this way, proper interpolation can be archived.

According to the above-described embodiments of the present invention, because sum data of plural important data are recorded, redundancy slightly increases due to the recording of the sum data. However, the redundancy is lower than when the same important data is recorded several times.

Another embodiment of the present invention will be described hereinafter. Fig. 16 shows an outline construction of an embodiment of a signal processing system for a digital VTR. Digital video signals are supplied from an input terminal 101. The digital video signals have been produced by quantizing one sample into eight bits, for example. The digital video signals are supplied to a block formatting circuit 102. In this embodiment, block formatting circuit 102 divides a valid area of one field or one frame into DCT blocks having (8×8) pixels.

Block formatting circuit 102 supplies to a DCT (Discrete Cosine Transform) circuit 103 the digital video signals which have been scan-converted in the order of the blocks. DCT circuit 103 generates coefficient data comprising one direct current component and sixty-three alternating current components. These coefficient data are supplied to a quantizing circuit 104. Quantizing circuit 104 re-quantizes the coefficient data by a predetermined quantizing step so that the number of bits of the data is reduced. Quantizing circuit 104 supplies its output to VLC (valuable length code) encoding circuit 105, whereby the supplied data are further compressed by the variable length encoding such as Run-length code or Huffman code.

Since the direct current component generated by DCT circuit 103 has higher importance for restoring an video of that block, it is transmitted directly without being processed by quantizing circuit 104 and VLC encoding circuit 105. A frame formatting circuit 106

constructs the direct current component, the variable length code from VLC encoding circuit 105, control data and ID data into data having continual synch blocks. While an error correction encoding is carried out in frame formatting in a conventional system, an error correction encoding is not necessary in the present invention.

Frame formatting circuit 106 supplies its output through a recording circuit 107 to a rotary head H so that the output is recorded on slant tracks on a magnetic tape T. Recording circuit 107 includes a channel encoding circuit, a recording amplifier and so on. The channel encoding is a process to reduce direct current component of record data. Although two or more rotary heads are normally used, only one head is shown in Fig. 16 for simplification.

Reproduced signals reproduced from magnetic tape T by rotary head H are supplied to a reproducing circuit 111 which comprises a reproducing amplifier, a channel decoding circuit and so on, so that the reproduced signals are channel-decoded thereby. The output data of reproducing circuit 111 is supplied to a frame deformatting circuit 112 so that various types of data are separated from the reproduced data. The output data of frame deformatting circuit 112 is supplied to a VLC decoding circuit 113 for decoding variable-length codes.

VLC decoding circuit 113 is connected to an inverse-quantizing circuit 114. Inverse-quantizing circuit 114 processes data in a manner reverse to quantizing process by quantizing circuit 104 at the recording side. The output data of inverse-quantizing circuit 114 is supplied to an inverse-DCT circuit 115. Inverse-DCT circuit 115 decodes the coefficient data so that (8×8) pixel data of a block are restored. The output data of inverse-DCT circuit 115 is supplied to a block deformatting circuit 116. Block deformatting circuit 116 changes the order of data from a block order to a raster-scan order. The output data of block deformatting circuit 116 is supplied to a correction circuit 117 embodying the present invention. An output data is derived from an output terminal 118 of correction circuit 117.

Fig. 17 shows an embodiment of correction circuit 117 according to the present invention. Reproduced data from block deformatting circuit 116 is supplied to an input terminal 121. The reproduced data is supplied to three-line memory 122 and the output data of three-line memory is supplied to a block formatting circuit 123. The output data of block formatting circuit 123 is supplied to an ADRC encoding circuit 124.

As shown in Fig. 19, block formatting circuit 123 forms block X1, next, block X2 and then block X3. Accordingly blocks which are shifted for one pixel in the horizontal direction are sequentially formed. Three-line memory 122 is provided to form the overlapping blocks. After blocks are formed over one line period, new blocks which shift for one line will be formed below them. A center pixel of each block is an pixel subject to error detection and error correction.

ADRC encoding circuit 124 detects for each block maximum data MAX and minimum data MIN of pixel data and dynamic range DR which is the difference between MAX and MIN. Pixel data are quantized adaptive to dynamic range DR. ADRC encoding circuit 124 generates 1-bit quantized data.

Fig. 20 shows an example of ADRC encoding circuit 124. In Fig. 20, regarding input data supplied from an input terminal 151, a detecting circuit 152 detects maximum data MAX and minimum data MIN for each block. MAX and MIN are supplied to a subtracting circuit 153 which generates dynamic range DR. The input data and MIN are supplied to a subtracting circuit 154. By subtracting the minimum data from subtracting circuit 154, normalized pixel data are generated.

Dynamic range DR is supplied to a dividing circuit 155 which divides the normalized pixel data by dynamic range DR. Quantized data DTX (for example, data up to three digits below radix point) are derived from an output terminal 158. In Fig. 19, DTX1, DTX2 and DTX3 are quantized data corresponding to blocks X1, X2 and X3, respectively. The output data of dividing circuit 155 is supplied to a comparing circuit 156. Comparing circuit 156 determines whether the divided output of eight pixels other than the center pixel are larger than or smaller than 0.5. According to this determination, data DT which is "0" or "1" are generated for each pixel. Data DT are derived from an output terminal 157.

Referring back to Fig. 17, the above-explained data DT included in the output data of 1-bit type ADRC encoding circuit 124 are supplied to a timing aligning circuit 125. Quantized data DPX are supplied to a selector 126 and comparing circuits 130 and 131. Timing aligning circuit 125 changes timings of data DT of eight pixels other than the center pixel of that block so that their timings become concurrent. The output data (eight bits) of timing aligning circuit 125; that is, class information, are supplied to a memory 129a as a read address.

Memory 129a stores range defining data (MAX^ and MIN^) for each class and representative data (DTx^) which have been predicted for each class. These data have been prepared by in-advance training, as explained later. The representative data are read out from memory 129a in accordance with the class information supplied from timing aligning circuit 125.

Representative data DTx^ which has been read out is supplied to a selector 126. MAX^ and MIN^ which have been read out are supplied to comparing circuits 130 and 131, respectively. The outputs of comparing circuits 130 and 131 are supplied to a logic circuit 132 which in turn generates a control signal to control selector 126. Comparing circuits 130 and 131

function as a window comparator. Where MAX^ < DTx < MIN^, quantized data DTx exists a range within which they should be. Therefore, it is determined that data DTx has no error. Where DTx < MIN or DTx > MAX^, it is determined that data DTx has an error.

If there is no error, selector 126 selects output data DTx of ADRC encoding circuit 124. If it is determined that there is an error, selector 126 selects data DTx^ read out from memory 129a. Accordingly, data DTx^ is selected in place of data which is determined to have an error. The selected output of selector 126 and DR and MIN from ADRC encoding circuit 124 are supplied to an ADRC decoding circuit 127.

Opposite to the above-explained encoding, ADRC decoding circuit 127 multiplies dynamic range DR and the output data of selector 126 and adds the result of the multiplying and minimum data MIN. Error-corrected output data are derived from an output terminal 128 of ADRC decoding circuit 127. In this manner, pixel data with an error can be corrected without using an error correction code.

Memory 129a stores the range defining data prepared by in-advance training and representative data predicted for each class. Fig. 18 shows a construction of the training. In Fig. 18, input digital video signals are supplied to an input terminal 141 and then, supplied to a block formatting circuit 143 through a three-line memory 142. The output of block formatting circuit 143 is supplied to an ADRC encoding circuit 144.

Three-line memory 142, block formatting circuit 143 and ADRC encoding circuit 144 are the same as three-line memory 122, block formatting circuit 123 and ADRC encoding circuit 124 in the above-explained correction circuit 117. However, it is preferable for the training that the input data is standard video data; for example, video signals composed of still picture videos of various texture (picture). Comparison output DT included in the output of ADRC encoding circuit 144 is supplied to a timing aligning circuit 145. Quantized data DTx is supplied to a memory 146a as input data. Like above-explained timing circuit 125, timing aligning circuit 145 makes the comparison outputs of eight pixels other than the center pixel of a (3×3) block a parallel data.

8-bit output of timing aligning circuit 145 is supplied to a memory 146a as write addresses. An address counter 147 generates read addresses for memory 146a. Write addresses for memory 146a are 8-bit class information supplied from timing circuit 145. For each of 256 classes, quantized data DTx which has been actually obtained for the center pixel is written onto memory 146a.

After the writing process is finished, data stored in memory 46a at each address (each class) is read out in accordance with a read address from address counter 147. The read address increments from 0 to 255. Data read out are supplied to an averaging circuit 148 and a detecting circuit 149. Averaging circuit 148 predicts representative data DTx^ for each class. Detecting circuit 149 detects maximum data of MAX^ and minimum data MIN^ of quantized data for each class.

The outputs of averaging circuit 148 and detecting circuit 149 are supplied to a memory 129a as input data and are written thereon at the address defined by the output of address counter 147. As a result of this training, memory 129a stores a class information defined by eight pixels in a 3x3 block, representative quantized data (DTx^) of that class and the range defining data of that class (MAX^, MIN^). As described above, memory 129 is used in correcting circuit 117.

Because Fig. 18 is used to show a principle of the training in a easy way, infinite data area for each address would be necessary and it would not be practical. Therefore, circuits as shown in Fig. 21 are actually used. 8-bit class information from timing aligning circuit 145 is supplied to a switching circuit 161. Quantized data DTx is supplied to comparing-and-selecting circuits 165 and 166 and an adding circuit 167.

Switching circuit 161 selects an output terminal $\underline{b}$ during the first half (reading period) of one block period and selects an output terminal $\underline{a}$ during second half (writing period). Write addresses from output terminal $\underline{a}$ of switching circuit 161 are supplied to a memory 146b. Output terminal $\underline{b}$ is connected to an input terminal $\underline{d}$ of a switching circuit 163. The output of address counter 162 is supplied to an input terminal $\underline{c}$ of switching circuit 163. Address counter 162 corresponds to address counter 147 as shown in Fig. 18. Switching circuit 163 selects read addresses from input terminal $\underline{d}$ during the training and selects read address from input terminal $\underline{c}$ after the training ends.

Memory 146b has maximum data, minimum data, accumulated data and count data CNT (count data CNT will be explained later) as input and output data. The accumulated data from memory 146b is supplied to an adding circuit 167 and a dividing circuit 168. The output of adding circuit 167 is input data to memory 146b. Accordingly, the accumulated data of quantized data of each class is input to memory 146b.

Comparing-and-selecting circuit 165 receives quantized data DTx and the minimum data from memory 146b, and selects and sends the smaller data to memory 146b. Comparing-and-selecting circuit 166 receives quantized data DTx and the maximum data from memory 146b, and selects and sends the larger data to memory 146b. Count data CNT is supplied to an adding circuit 164 and +1 is added thereby. The added data is input to memory 146b.

Writing operation of memory 146b is carried out after reading operation thereof. According to the above circuits, when the training period ends, memory 146b stores the accumulated data of quantized data, the maximum data, the minimum data and frequency of the happening for every class. After the training, switching circuit 163 changes its selection

so that incrementing addresses from address counter 162 are supplied to memory 146b and memory 129 as read address and write address, respectively.

An dividing circuit 168 divides the accumulated data from memory 146b by count data CNT. Therefore, dividing circuit 168 outputs average data, that is, predicted quantized data DTx^ and DTx^ is written in memory 129b. The maximum data and minimum data from memory 146b are written into memory 129b as range defining data MAX^ and MIN^. By using the circuits as shown in Fig. 21, it can be avoided that data area necessary for each address becomes infinite.

Next, another embodiment of the present invention will be described. An overall construction of a recording circuit and reproducing circuit in the another embodiment is the same as shown in Fig. 16. Fig. 22 shows another embodiment of correcting circuit 117. Circuit blocks corresponding to the above-explained embodiment of correcting circuit 117 (Fig. 17) will have the same reference numerals. Through an training which will be described later, memory 129c stores weighting factor data $\omega 1$ - $\omega 8$ and allowance data σ for errors.

A block formatting circuit 123 sequentially forms blocks of 3×3 pixels (Pixel data in a block are shown by a-i). Actual data e of its center pixel is supplied to a comparing circuit 171 and a selector 175. The eight pixel data other than the center pixel data are supplied to an ADRC encoding circuit 124 and an operating circuit 172. Although ADRC encoding circuit 124 is the same as shown in Fig. 20, it generates only comparison output DT of eight pixels. A timing aligning circuit 125 which is connected to ADRC encoding circuit 124 forms 8-bit class data which is supplied to a memory 129c as a read address.

Weighting factor data $\omega 1$ - $\omega 8$ from memory 129c are supplied to operating circuit 172. Operating circuit 172 generates a predicted data e^ of the center pixel e as follows :

$$e^ = \omega 1a + \omega 2b + \omega 3c + \cdots + \omega 8i$$

Predicted data e^ from operating circuit 172 and error allowance data σ are supplied to an adding circuit 173 which generates $e^ + \sigma$. Predicted data e^ from operating circuit 172 and error allowance data σ are supplied to a subtracting circuit 173 which generates $e^ - \sigma$. The output data of adding circuit 173 and subtracting circuit 174 are supplied to a comparing circuit 171.

Comparing circuit 171 determines that there is no error when $e^ - \sigma < e < e^ + \sigma$. It determines that there is an error, otherwise. Comparing circuit 171 generates a control signal to a selector 175. When there is no error, selector 175 selects actual data e. When there is an error, selector 175 selects predicted data e^. Selector 175 generates a corrected output data from its output terminal 176.

Fig. 23 shows a training circuit to store necessary data in memory 129c. For the training purpose, digital video signals of standard pictures are supplied to an input terminal 141. Circuit blocks corresponding to those as shown in Fig. 18 will have the same reference numerals. A block formed by a block formatting circuit 143 composes of pixel data a - i, as shown in Fig. 23. Data of each block are supplied to an ADRC encoding circuit 144, an identifying circuit 177 and an error operating circuit 178. 8-bit class data from a timing circuit 144 and sequential addresses from an address counter 147 are supplied to identifying circuit 177.

Identifying circuit 177 identifies weight factors $\omega 1$ - $\omega 8$ in such a manner that the sum of squares of errors becomes the least by using a least-squares method. Identifying circuit 177 has a data memory. In this data memory, pixel data in a block are stored at an address which is class information. For example, at an address corresponding to one class, (a1, a2, ---, an) for pixel data a, (b1, b2,----, bn) for pixel data b, (c1, c2, ---, cn) for pixel data c --- and (i1, i2 ----, in) for pixel data for i are stored. At other addresses corresponding to other classes, pixel data are similarly stored.

Next, by a least-square method using the stored data, weighting factor data $\omega 1$ - $\omega 8$ to minimize error are calculated. Paying attention to one class, the following equations can be made for this class.

$$e1 = \omega 1a1 + \omega 2b1 + \omega 3c1 + \cdots + \omega 8i1$$
$$e2 = \omega 1a2 + \omega 2b2 + \omega 3c2 + \cdots + \omega 8i2$$
$$\vdots$$
$$en = \omega 1an + \omega 2bn + \omega 3cn + \cdots + \omega 8in$$

Because a1 - an, b1 - bn, --- and i1 - in are known here, weighting factors $\omega 1$ - $\omega 8$ to minimize a sum of squares of errors with respect to actual data e1 - en can be calculated. The same calculations are carried out for other classes. $\omega 1$ - $\omega 8$ for each class calculated by identifying circuit 177 are sequentially written in memory 129c at addresses from address counter 147.

Error operating circuit 178 operates identified weighting factors $\omega 1$ - $\omega 8$ and actual data in a block other than e and generates predicted data e^. Error operating circuit 178 calculates an error between actual data e and predicted data e^. The calculation to detect the error is carried out for every class. Regarding one class, the following plural error data Ei are calculated

$$E1 = e^1 - e1$$
$$E2 = e^2 - e2$$
$$\vdots$$
$$En = e1an - en$$

The output data E1 - En of error operating circuit 178 are supplied to a detecting circuit 179. Detecting circuit 179 detects maximum MAX and minimum MIN

of error of each class. The output of detecting circuit 179 is supplied to a multiplying circuit 180. A predetermined coefficient N (where $0 < N < 1$) is supplied to an input terminal 181 of multiplying circuit 180. Multiplying circuit 180 carries out the following calculation to generate error allowance data σ.

$$\sigma = (MAX - MIN) \times N/2$$

It is preferable that the value of N is chargeable.

Data σ generated by multiplying circuit 180 are sequentially written in a data area at each address in memory 129c. By the above training, weighting factors $\omega 1$ - $\omega 8$ and error allowance data σ are respectively stored in a data area at each address. Memory 129c is then used in the correcting circuit as shown in Fig. 22. By using data stored in memory 129c, the detection of whether there is an error and the correction thereof are possible.

Referring to Fig. 24, a further embodiment of the present invention will be described. In the above-explained correction circuit as shown in Fig. 22, allowance data σ read out from memory 129c is fixed. The further embodiment has a learning function in which σ varies in accordance with frequency of a error. In Fig. 24, circuit blocks corresponding to those of Fig. 24 will have the same reference numerals.

Allowance data σ read out from memory 129c is supplied to anadding circuit 173 and a subtracting circuit 174 through a multiplying circuit 182. Multiplying circuit 182 is a circuit to vary σ. As described above, comparing circuit 171 generates a 1-bit output signal which shows whether a reproduced pixel data e has an error. This output signal is supplied to a counter 183 which counts the output signal (for example, "1") showing the existence of an error. Although not shown in Fig. 24, counter 183 is reset every line.

As shown in Fig. 25, block formatting circuit 123 sequentially forms blocks of 3×3 pixels. Counter 183 counts errors for plural blocks composed of three line of pixel data. A latch 184 latches the count of counter 183 and the output of latch 184 is supplied to a ROM 185 as a read address. ROM 185 generates coefficient K ($0 < K \leq 1$) for varying σ. Coefficient K is supplied to multiplying circuit 182. Multiplying circuit 182 generates $K\sigma$ which is used for processing next one line.

A table stored in ROM 183 has a characteristic that when there are fewer errors, K is a small number, and that when there are many errors, K is a bigger number. When there are fewer errors, reproduced data is used more often by narrowing error allowance σ. On the other hand, when there are many errors, data correction is made more often by widening error allowance σ. This results in the improvement of reproduced video quality.

Unlike the above embodiment of the correcting circuit, the training may be done regarding DCT coefficient and the correction may be done by using the DCT coefficient. As a block encoding to compress the amount of recording data, ADRC, vector-quantization and so on other than DCT may be used.

As described above, errors of received or reproduced video data can be corrected without using an error correction code. Accordingly, an increase in redundancy of transmitted data can be avoided. As shown in Fig. 26, there is extremely high probability of that actual data of each class exists around the representative quantized data as the center and exists within a range between maximum data MAX and minimum data MIN which had been prepared for every class through the training. Therefore, the error correction can be achieved with high accuracy.

Claims

1. A data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein said block code data includes important data which has high importance for decoding purpose, said transmission apparatus being characterized in that:

   a sum data of said plural important data is formed;

   said sum data is transmitted in time and space different from that of said plural important data; and

   said plural important data are restored from received said sum data and received said plural important data.

2. A data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein said block code data includes important data which has high importance for decoding purpose and wherein said block code data is transmitted in plural channels, said transmission apparatus being characterized in that:

   a sum data is formed by operating a plurality of said important data fewer than the number of said channels;

   said sum data is transmitted in a channel other than channels for transmission of said important data constituting said sum data; and

   said plural important data are restored from received said sum data and received said plural important data.

3. A data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space

is encoded as a unit of encoding to compress a data amount for the transmission, wherein said block code data includes important data which has high importance for decoding purpose, said transmission apparatus being characterized in that:

a weighted average data is formed for said plural important data;

said weighted average data is transmitted in time and space different from that of said plural important data; and

said plural important data are restored from received said weighted average data and received said plural important data.

4. A data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein said block code data includes important data which has high importance for decoding purpose, said transmission apparatus being characterized in that: a sum data is formed for a unit of said plural important data by operating said plural important data in that unit and at least one important data in another unit;

said sum data is transmitted in time and space different from that of said plural important data; and

said plural important data are restored from received said sum data and received said plural important data.

5. A data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein said block code data includes important data which has high importance for decoding purpose, said transmission apparatus being characterized in that: a sum data is formed for a unit of said plural important data by operating said plural important data in that unit and at least one important data in another unit, wherein a type of said plural important data changes regularly;

said sum data is transmitted in time and space different from that of said plural important data; and

said plural important data are restored from received said sum data and received said plural important data.

6. A data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein said block code data includes plural data, said transmission apparatus being characterized in that:

a sum data of said plural data is formed;

said sum data is transmitted in time and space different from that of said plural data;

when one of received said sum data and received said plural data has an error, the data having an error is restored from said sum data and the remaining plural data having no error;

when a plurality of received said data have errors, an interpolated data is formed by interpolating the data having an error in space or in time; and

the errors of said received plural data are corrected based upon said interpolated data and said sum data.

7. A data transmission apparatus for transmitting block code data generated by block encoding in which a block of plural pixels proximate in space is encoded as a unit of encoding to compress a data amount for the transmission, wherein said block code data includes plural data, said transmission apparatus being characterized in that:

a sum data is formed by adding bit data from MSB to a predetermined bit position with respect to said plural data;

said sum data is transmitted in time and space different from that of said plural data; and

said plural data are restored from received said sum data and received said plural data.

8. A data transmission apparatus for transmitting digital video signals, having error detecting means for detecting errors of received or reproduced digital video signals, said error detecting means comprising:

clustering means for clustering based upon plural pixel signals proximate in space or in time to a pixel to be detected;

memory means for storing existing-range data which has been provided in advance by training for each class;

reading means for reading out said existing-range data for a class corresponding to an address data which is defined by an output of said clustering means; and

comparing means for comparing an output of said reading means and pixel data of the pixel to be detected, whereby whether an error exist or not is detected based upon an output of said comparing means.

9. A data transmission apparatus according to claim 8, wherein said memory means further stores information regarding representative data for each class, and wherein the pixel data to be detected

is substituted with representative data formed based upon the information regarding representative data when the existence of an error is detected based upon the output of said comparing means.

10. A data transmission apparatus according to claim 8, wherein the reproduced or received digital video signals are encoded video signals, said apparatus further comprising decoding means for decoding the encoded video signals, and said clustering means clustering based upon decoded outputs of plural pixel data proximate to the pixel data to be detected.

11. A data transmission apparatus according to claim 8, wherein the encoded video signals are made by variable-length encoding a coefficient data obtained by DCT.

12. A data transmission apparatus according to claim 8, wherein said clustering means comprises ADRC encoding means and is supplied with the pixel data to be detected and the plural pixel data proximate thereto, and wherein among the encoded data the encoded data corresponding to the plural pixel data are used as a class information.

13. A data transmission apparatus according to claim 8, wherein the existing-range defining data is the maximum and minimum of actual data detected for each class.

14. A data transmission apparatus according to claim 8, wherein the information regarding representative data is an average of actual data detected for each class.

15. A data transmission apparatus according to claim 8, wherein the existing-range defining data is a coefficient data which is operated with the plural proximate pixel data, and an error allowance information.

16. A data transmission apparatus according to claim 9, wherein the information regarding representative data is a coefficient data which is operated with the plural proximate pixel data and wherein the representative data results from the operation of the coefficient data and the plural proximate pixel data.

17. A data transmission apparatus according to claim 15, further comprising counter means for counting the number of pixels having detected errors in a certain period and wherein the error allowance information can vary in accordance with an output of said counter means.

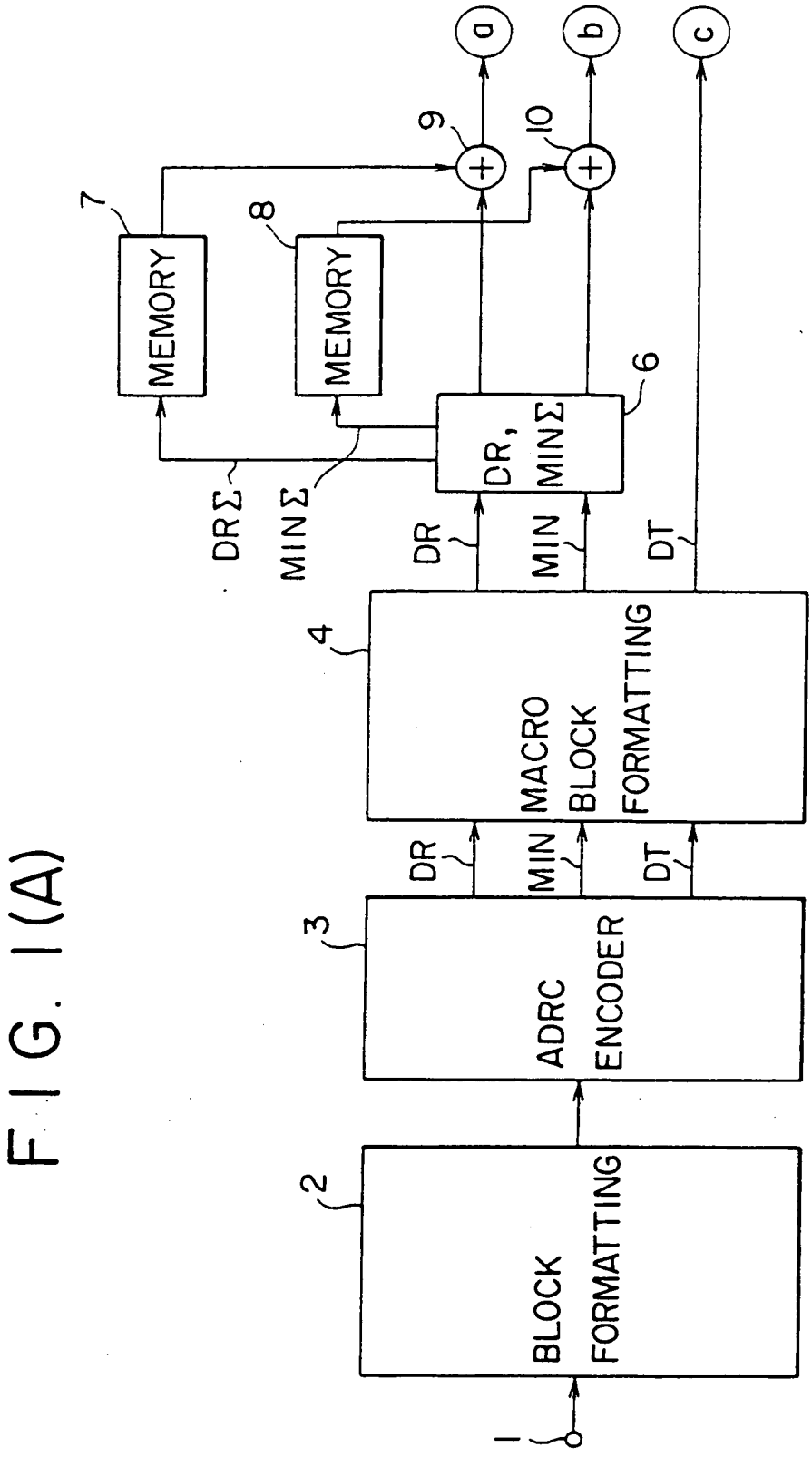


FIG. 1(A)

FIG. 1

FIG. 1(A)	FIG. 1(B)

FIG. 1(B)

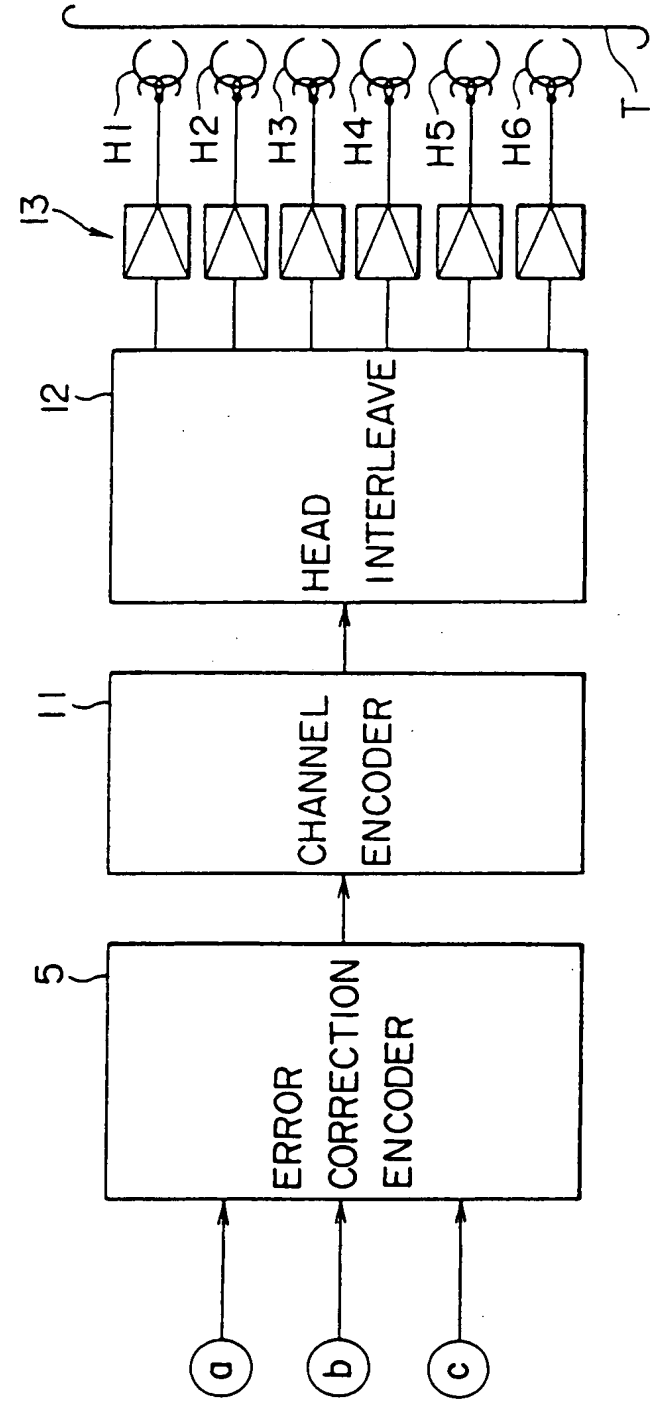


FIG. 2

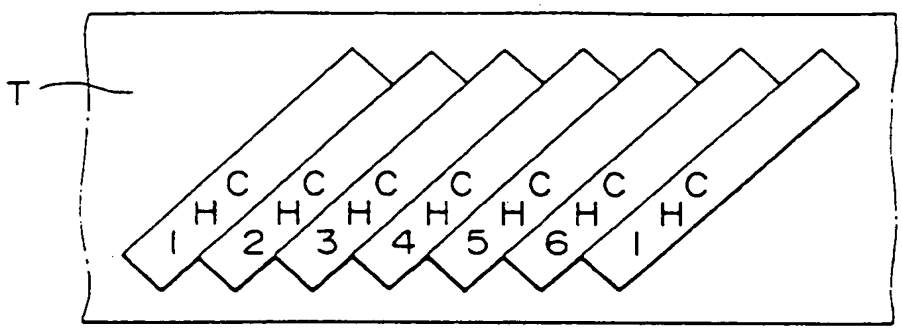


FIG. 3

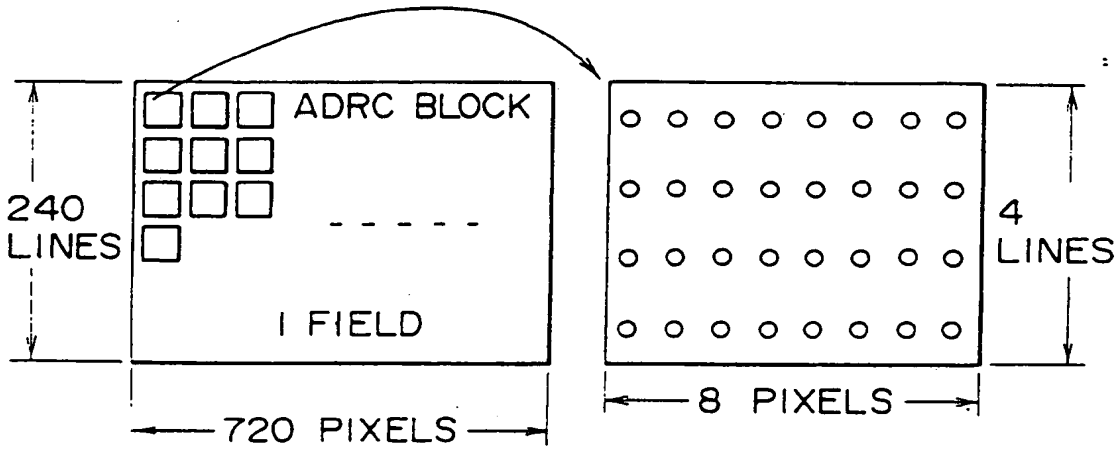


FIG. 4

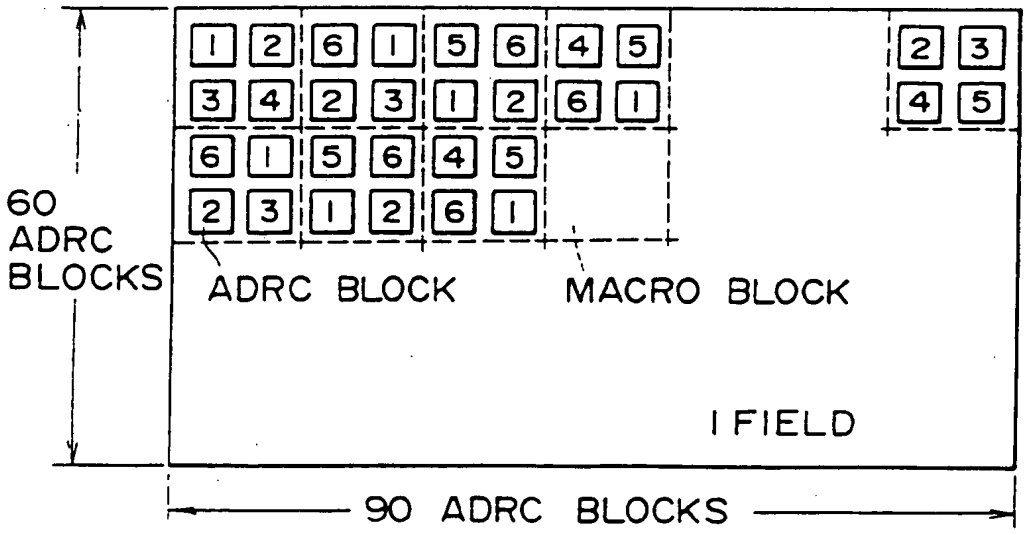


FIG. 5

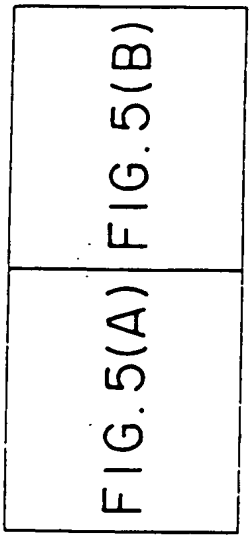
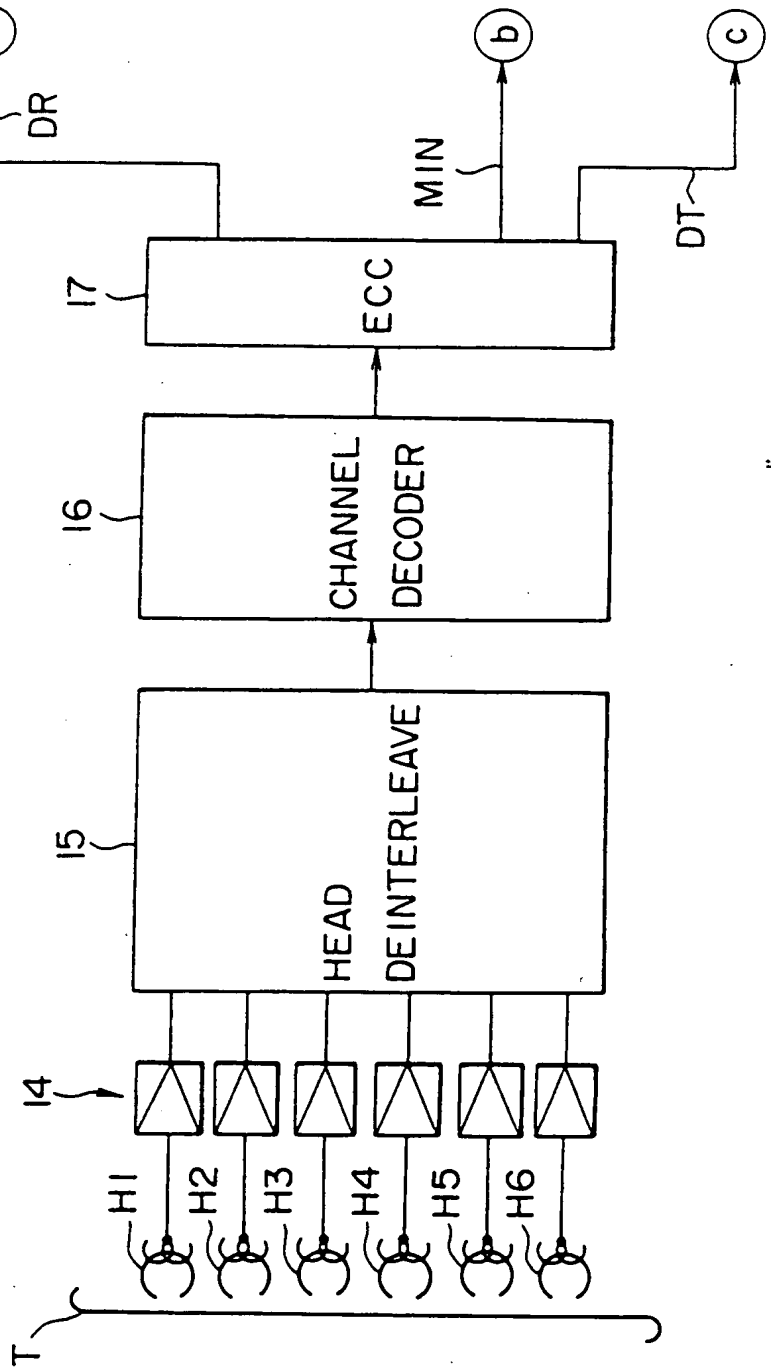
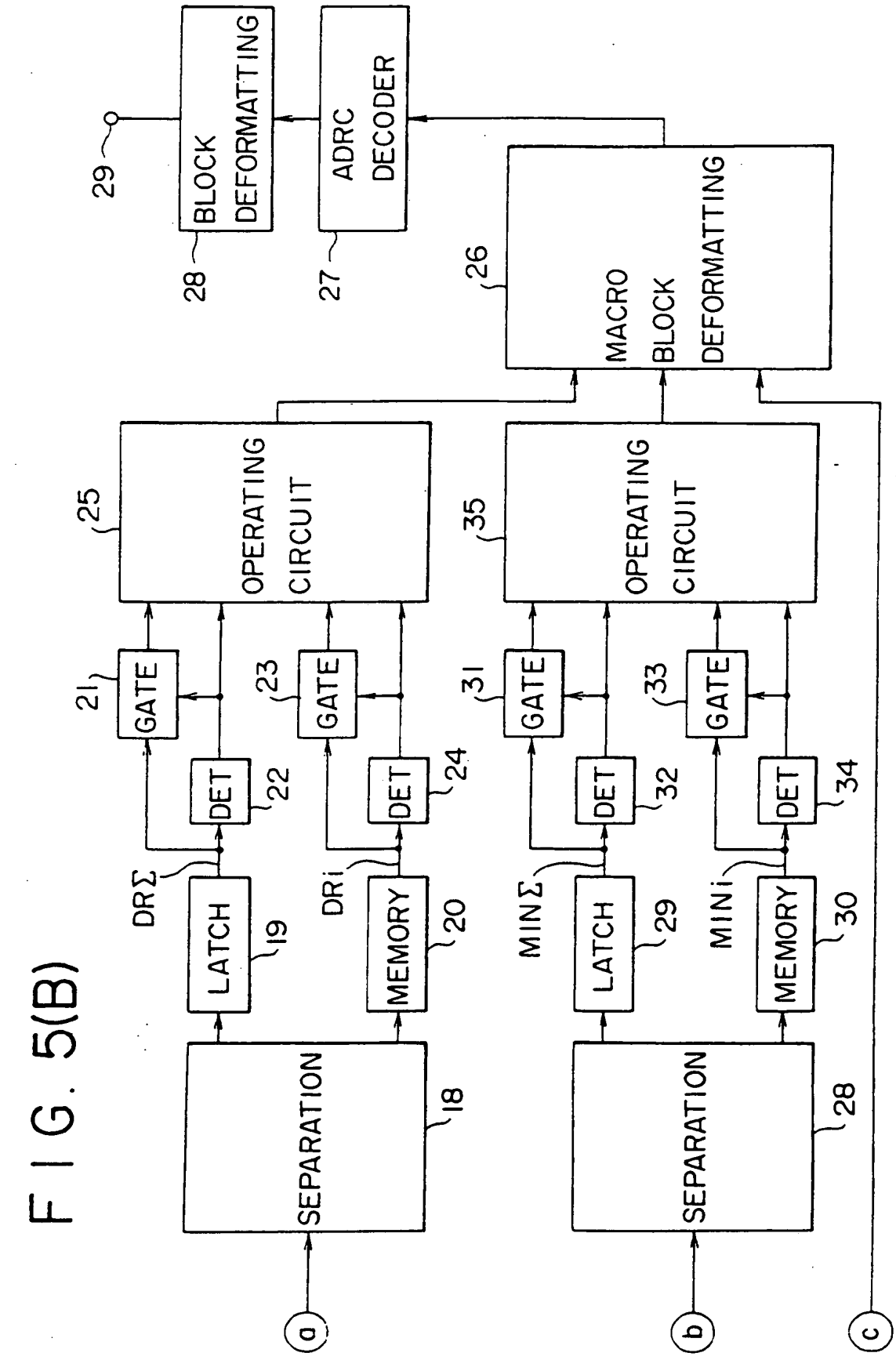


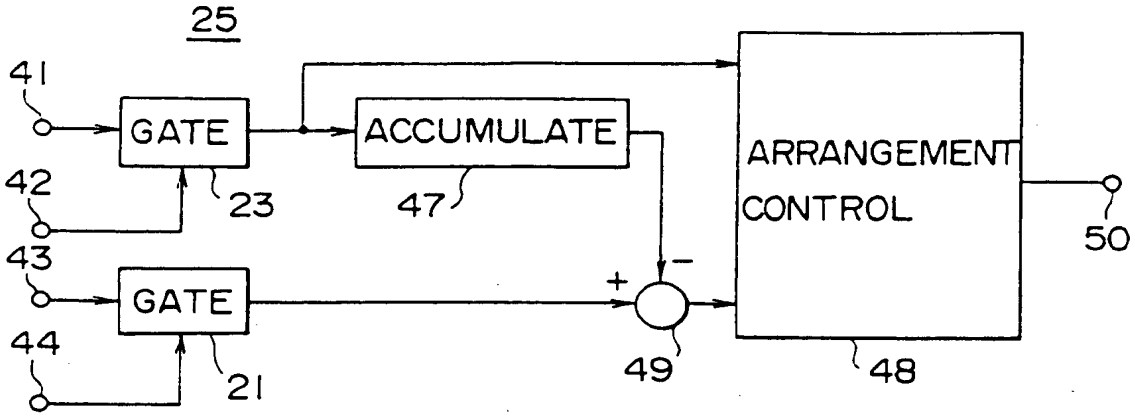
FIG. 5(A)





F I G. 5(B)

FIG. 6



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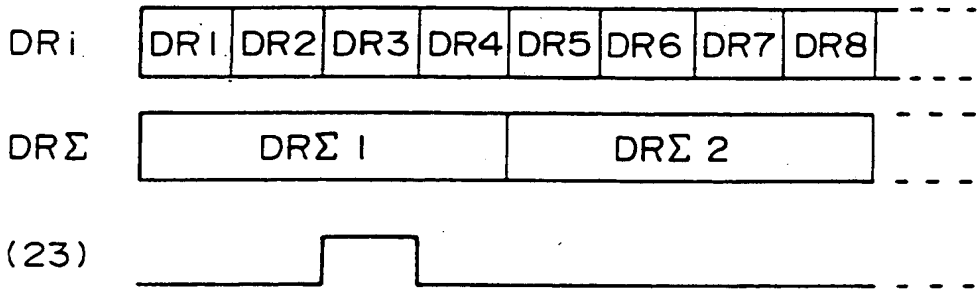


FIG. 8

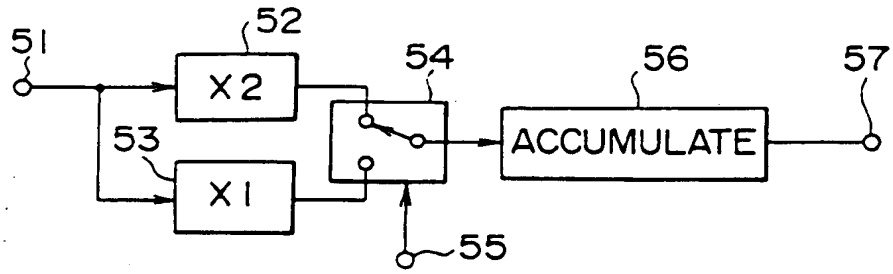


FIG. 9

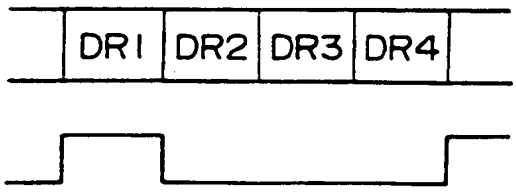


FIG. 10

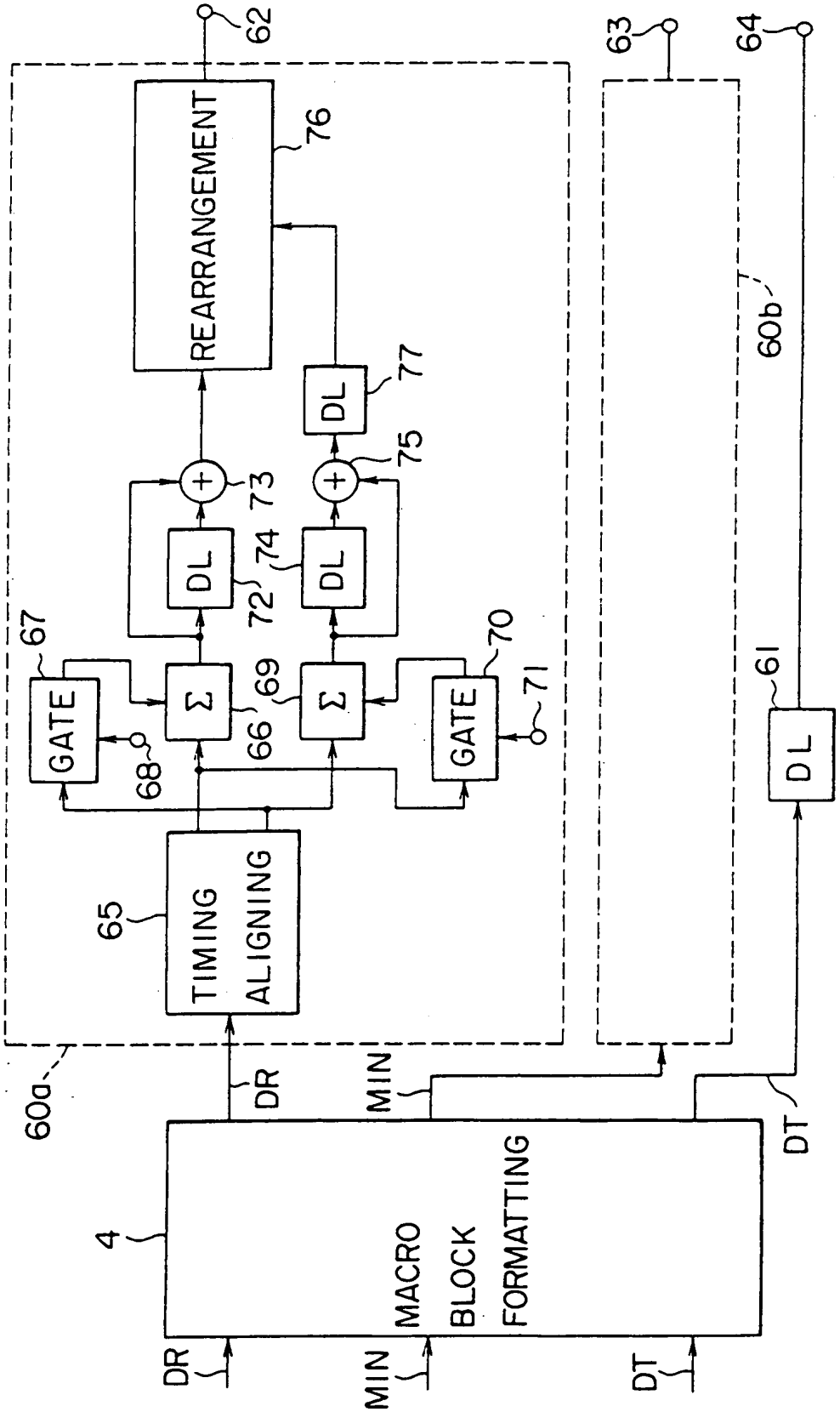


FIG. 11

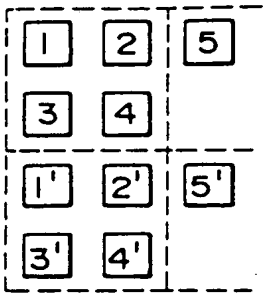


FIG. 12

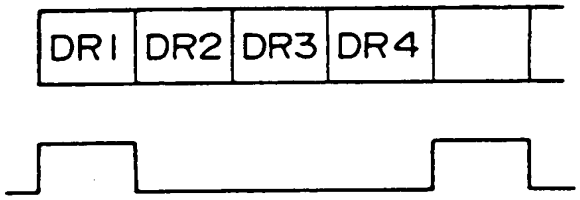


FIG. 13

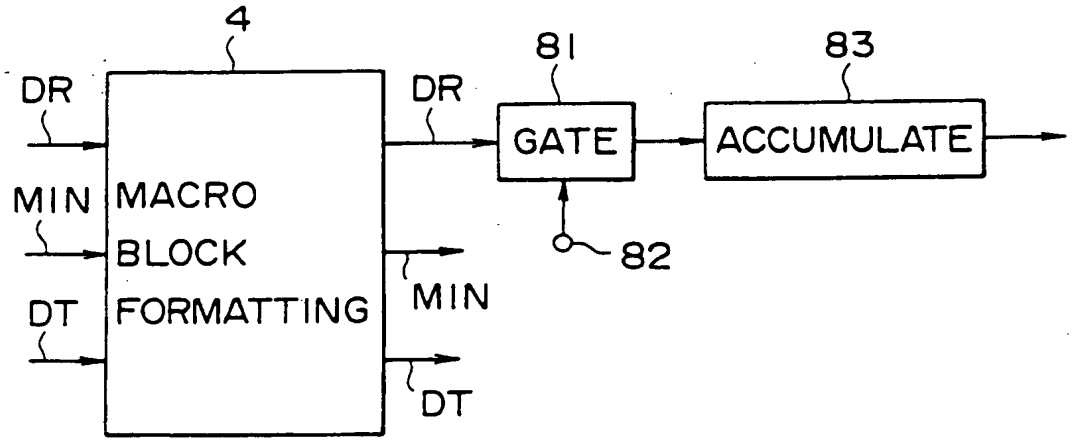
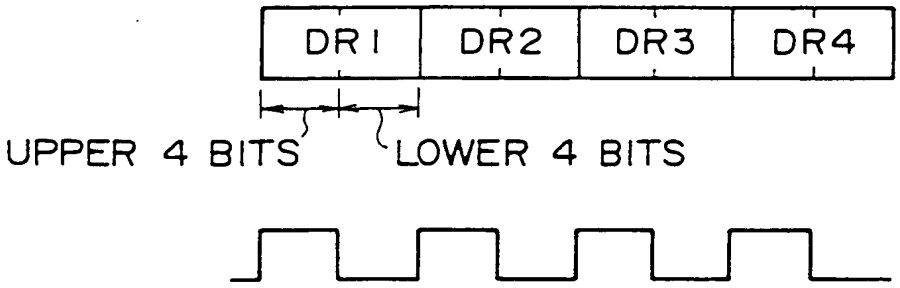


FIG. 14



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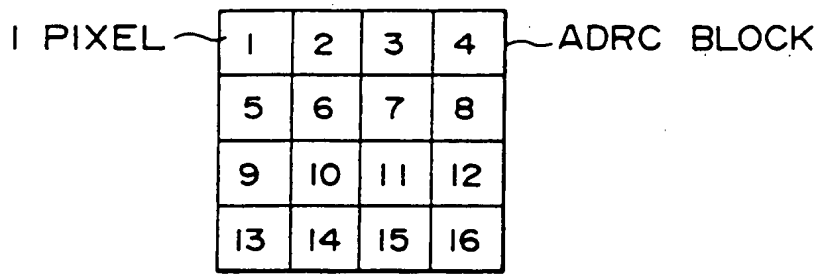


FIG. 16

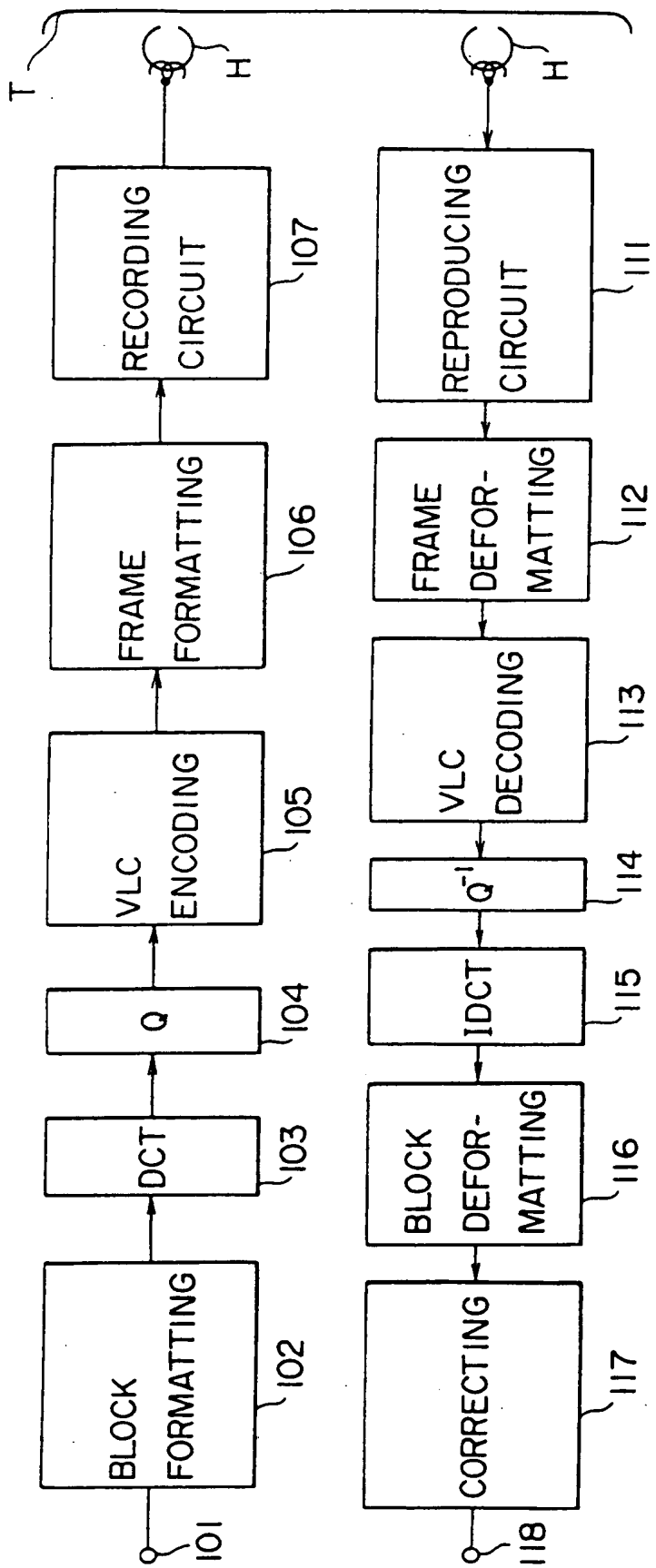


FIG. 17

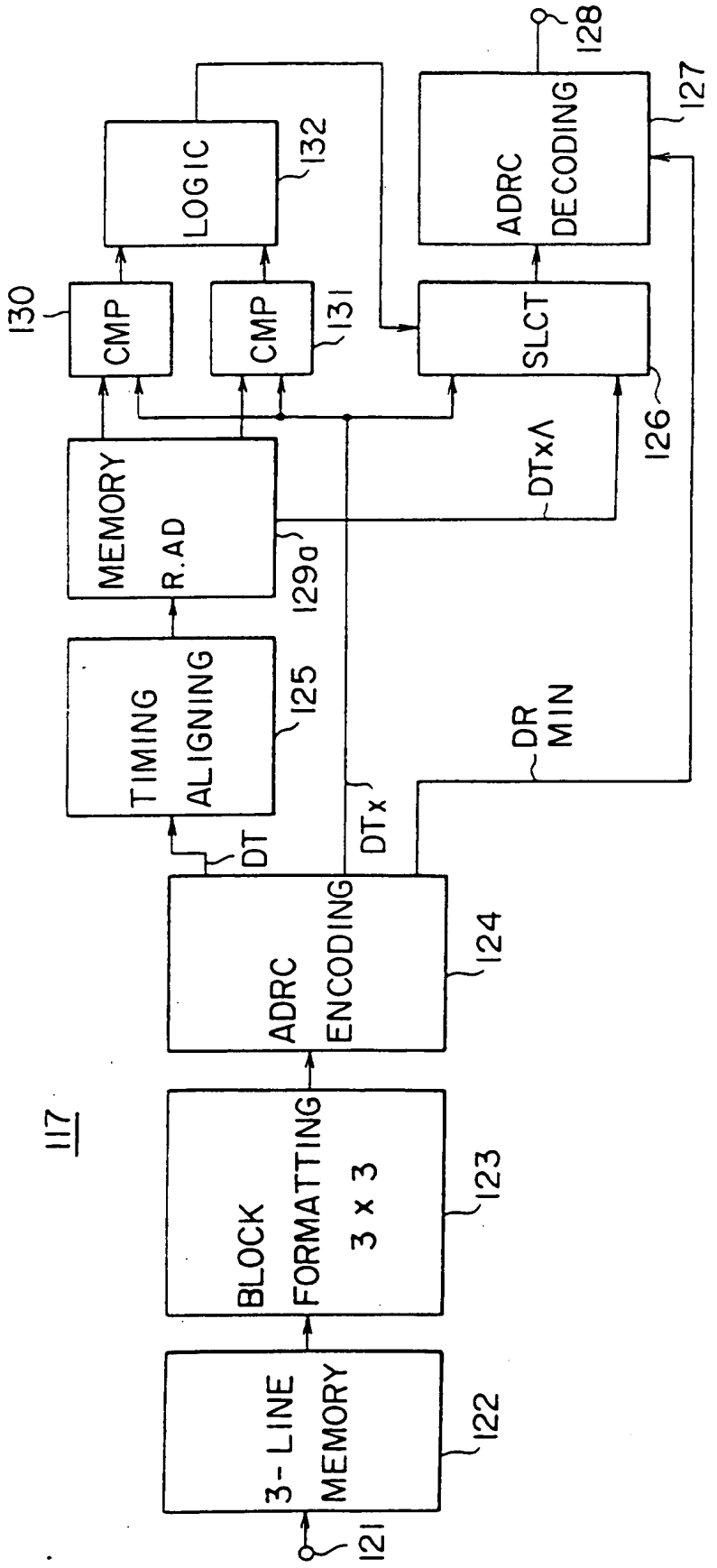


FIG. 18

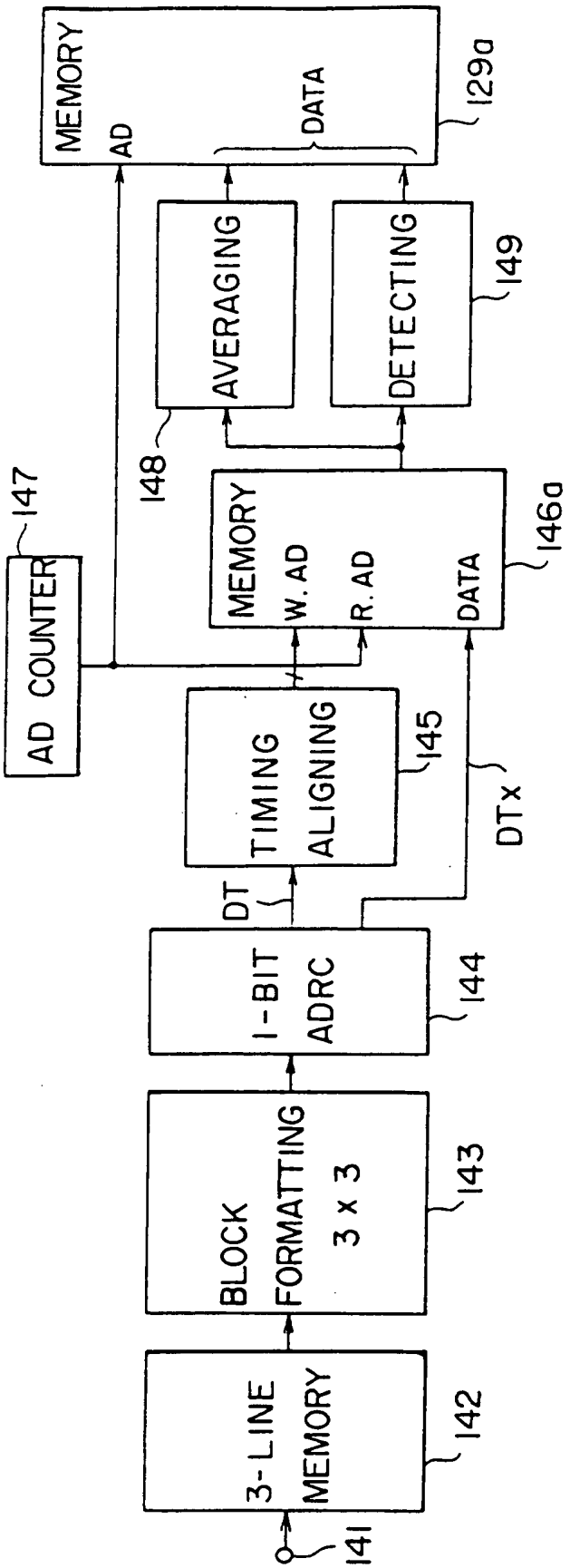


FIG. 19

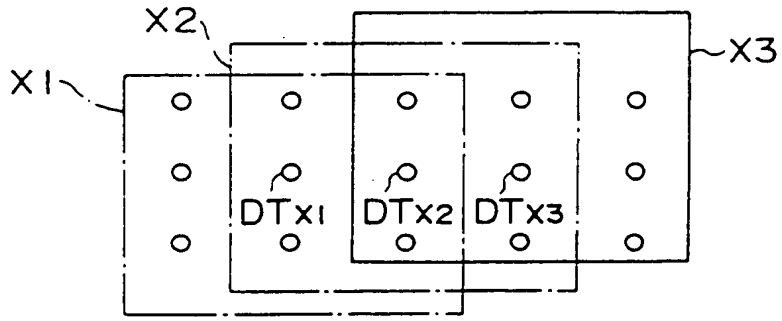


FIG. 20

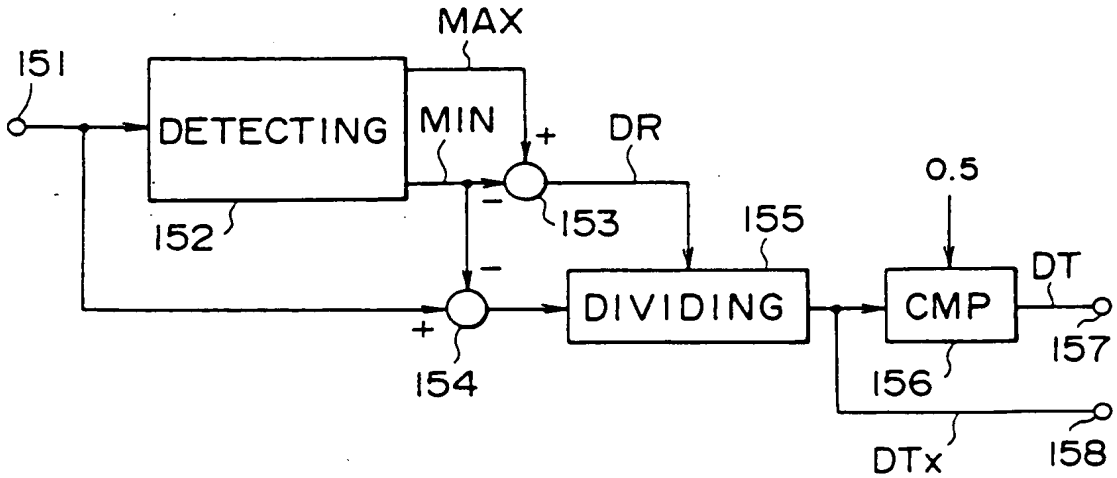


FIG. 21

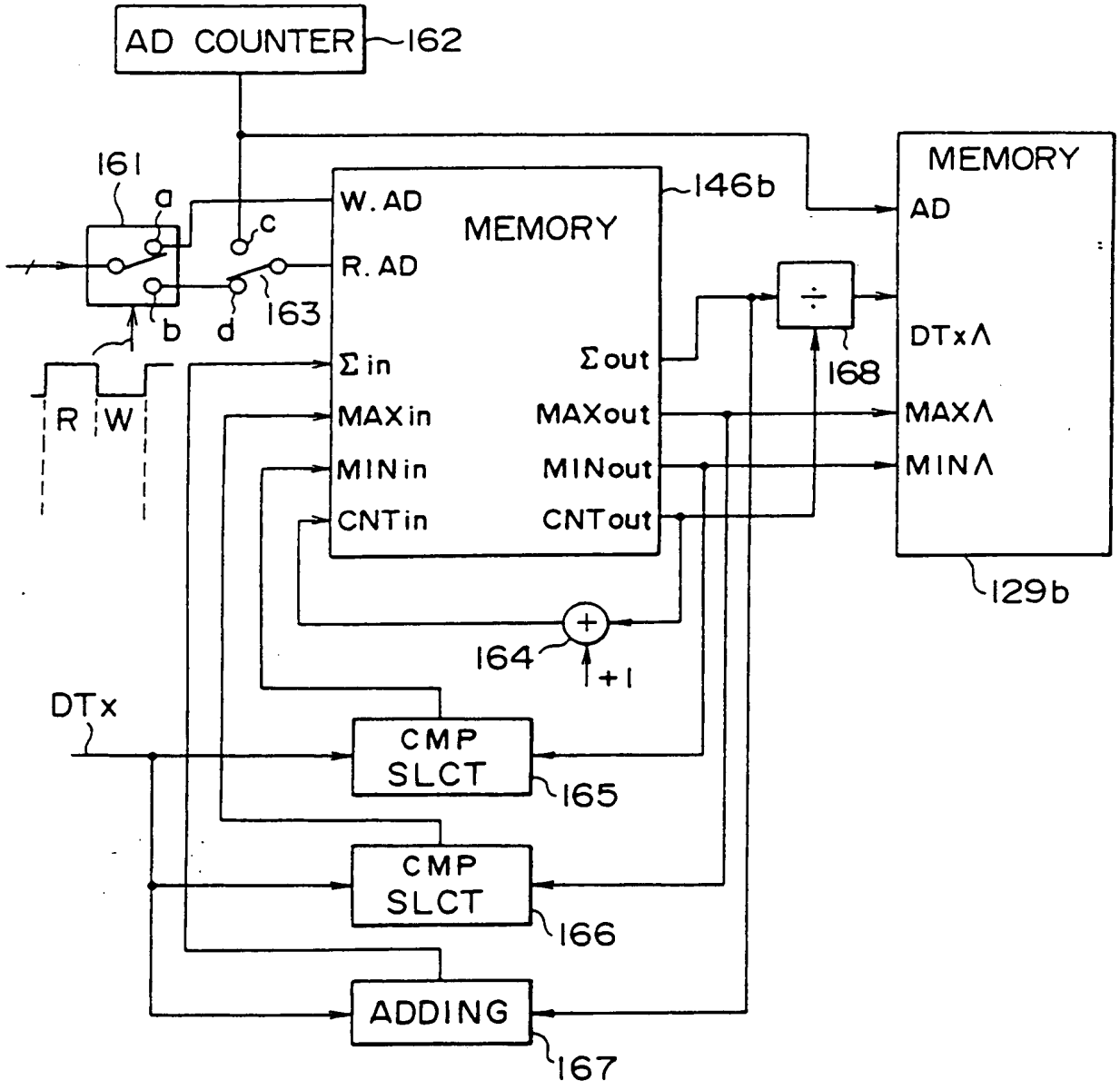


FIG. 22

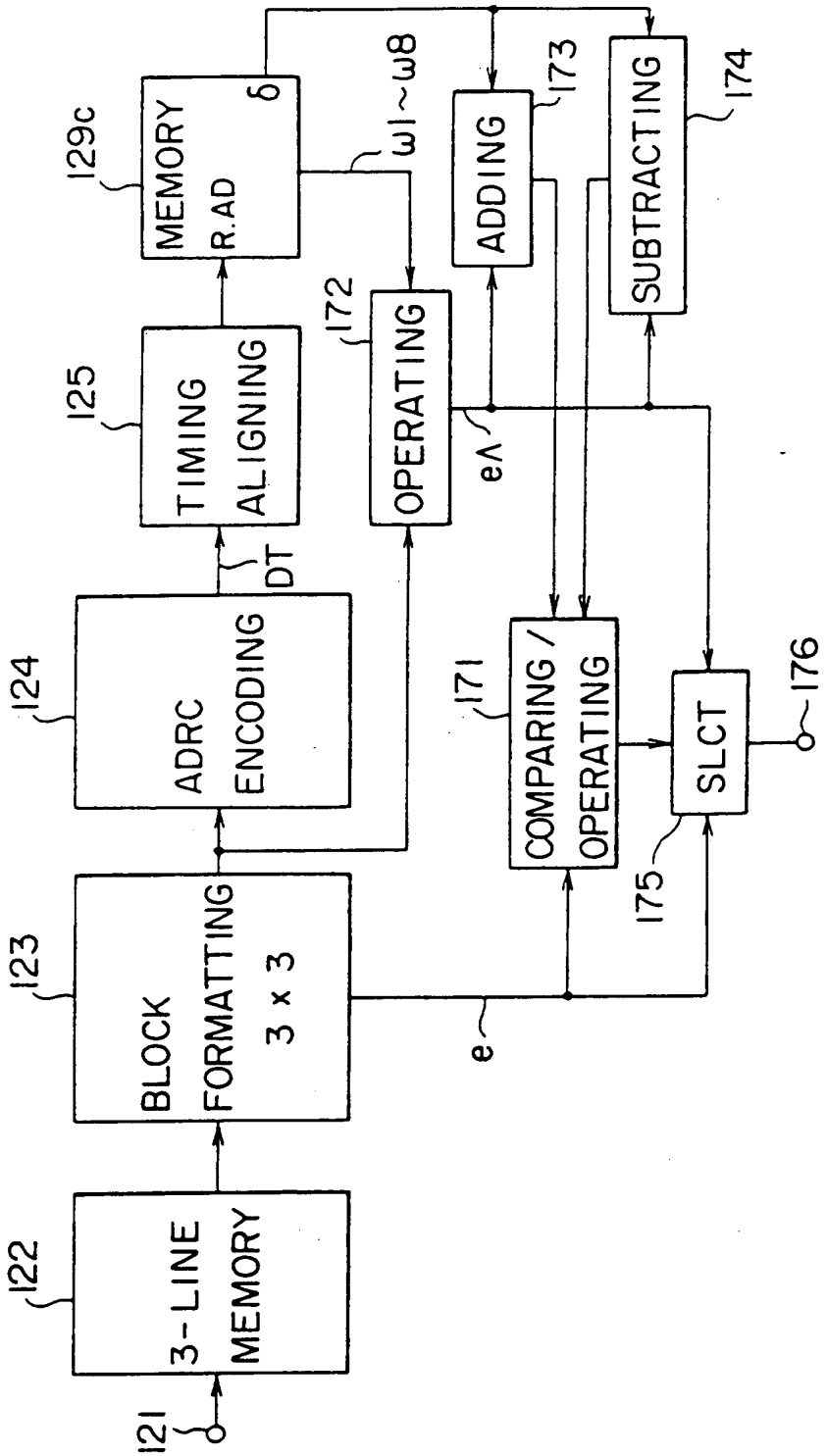


FIG. 23

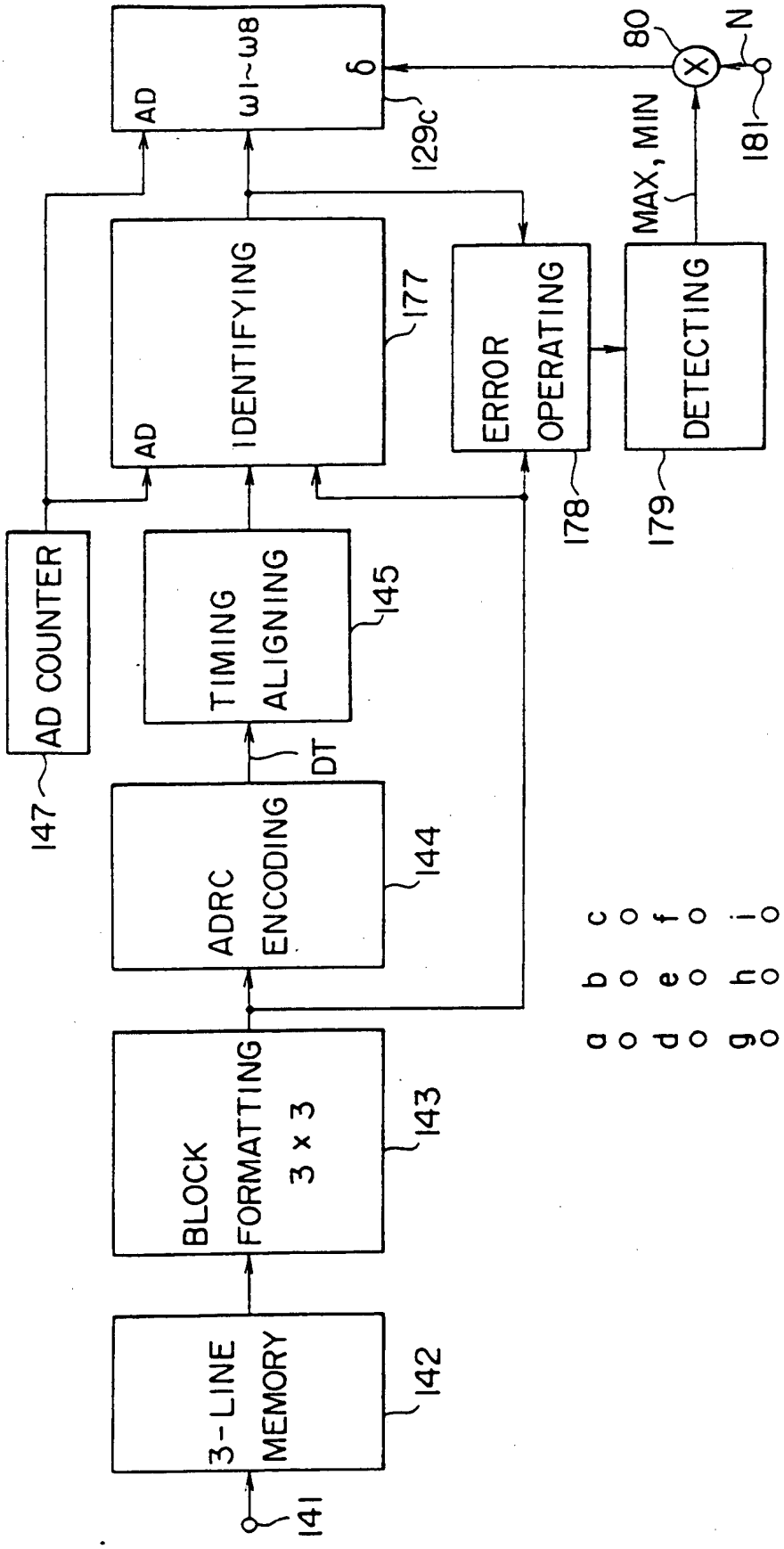


FIG. 24

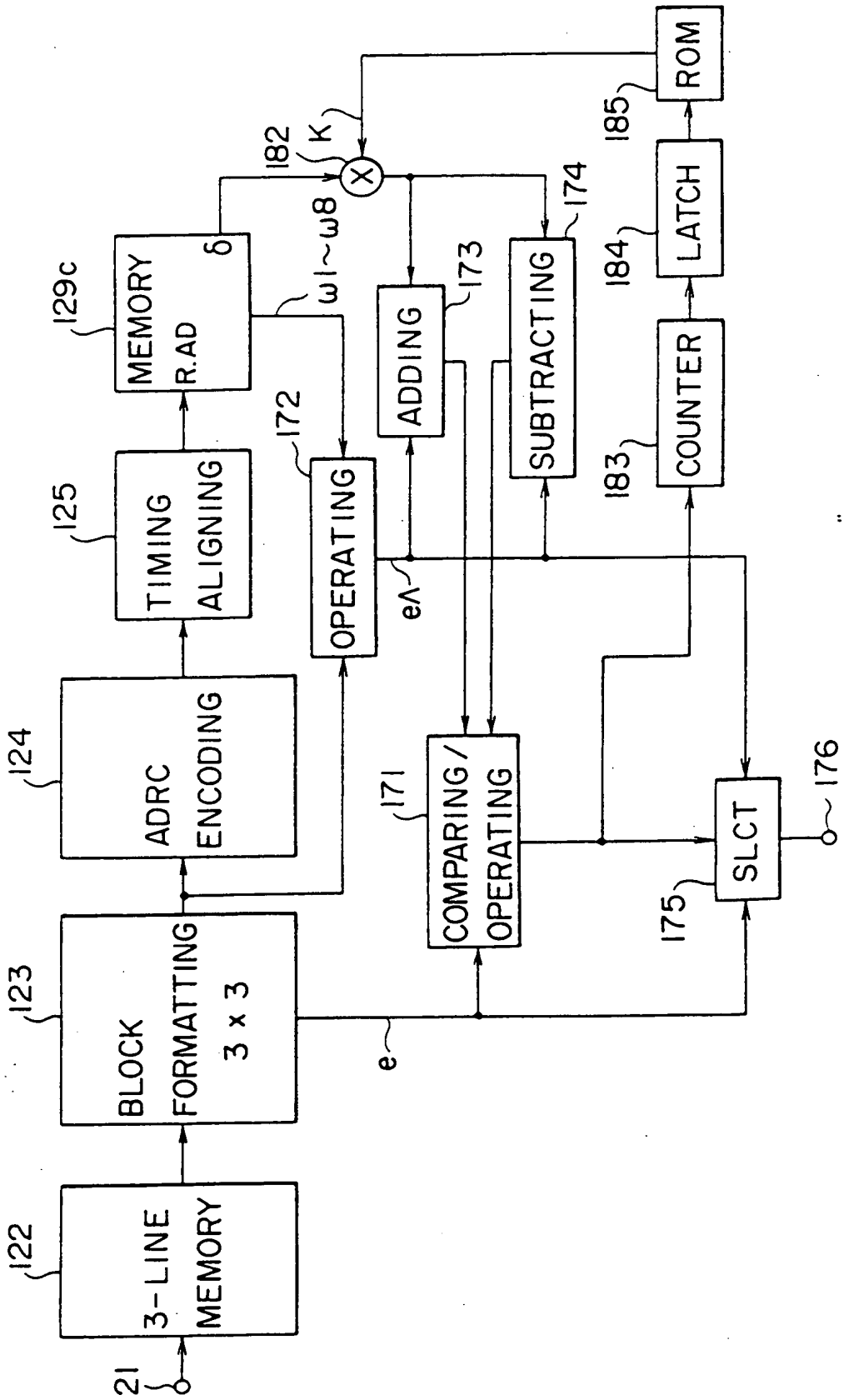


FIG. 25

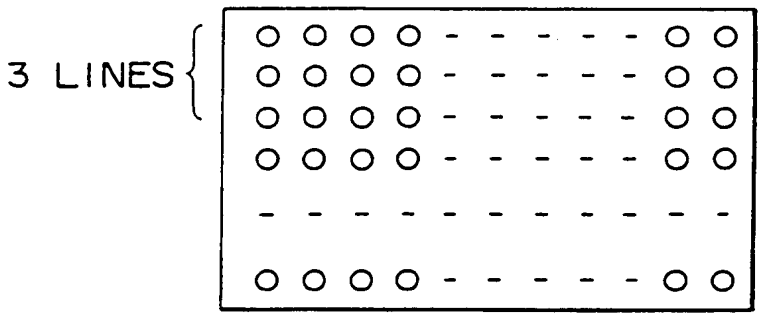
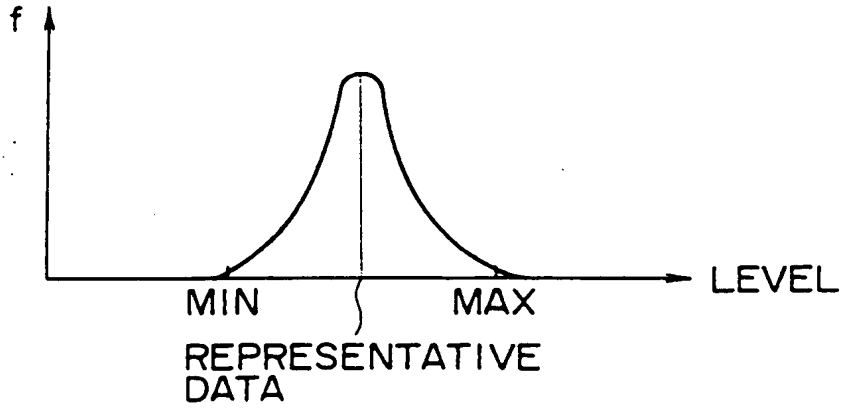


FIG. 26



(19) Europäisches Patentamt
European Patent Office
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(11) EP 0 597 576 A3

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(43) Date of publication A2:
18.05.1994 Bulletin 1994/20

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(54) Data transmission apparatus

(57) An ADRC encoder generates, regarding an ADRC block of 4x4 pixels, DR, MIN and quantized data corresponding to each pixel. A macro block formatting circuit generates code data DR, MIN and DT of four ADRC blocks. An adding circuit generates sum data (DR =DR1 + DR2 + DR3 + DR4, same calculation regarding MIN) of important data in the macro block. Mixing circuits insert the sum data into recording data as additional data. The sum data and the important data are distributed and recorded in plural channels. If one of the important data has an error and the remaining important data and the sum data have no error, the important data with the error can be completely corrected. Error correction of the important data and the quantized data generated by block encoding is effected with restrained increase in redundancy. Input data which has been reproduced and DCT-decoded is supplied to and is converted into 3x3 block format by a 3-line memory and block formatting circuit . An ADRC encoding circuit generates encoded data DTx of a center pixel data and data DT which is made up of peripheral 8 pixel data. A timing aligning circuit generates class information comprising 8 pixel data and the class information is supplied to a memory as a read address. Memory stores existing-range data and predicted data DTx^ through in-advance training. An error is detected by comparing the existing-range data and reproduced data DTx and when there is an error, predicted data DTx is selected. Error correction of received or reproduced image data is effected without using an error correction code.

FIG. 5

FIG. 5(A) FIG. 5(B)

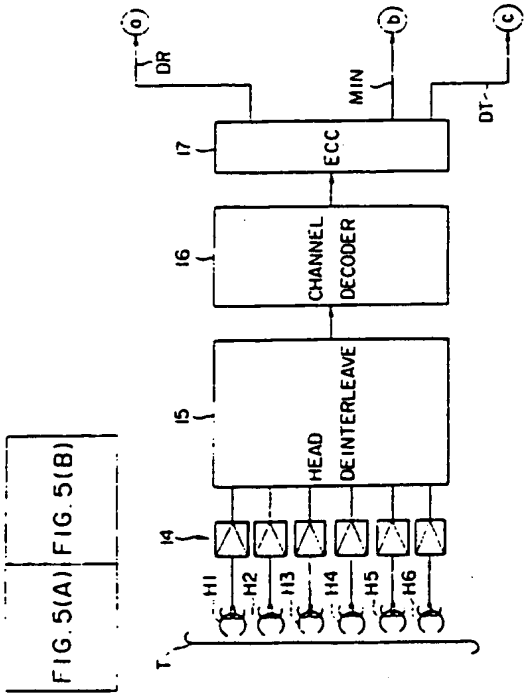

FIG. 5(A)

EP 0 597 576 A3

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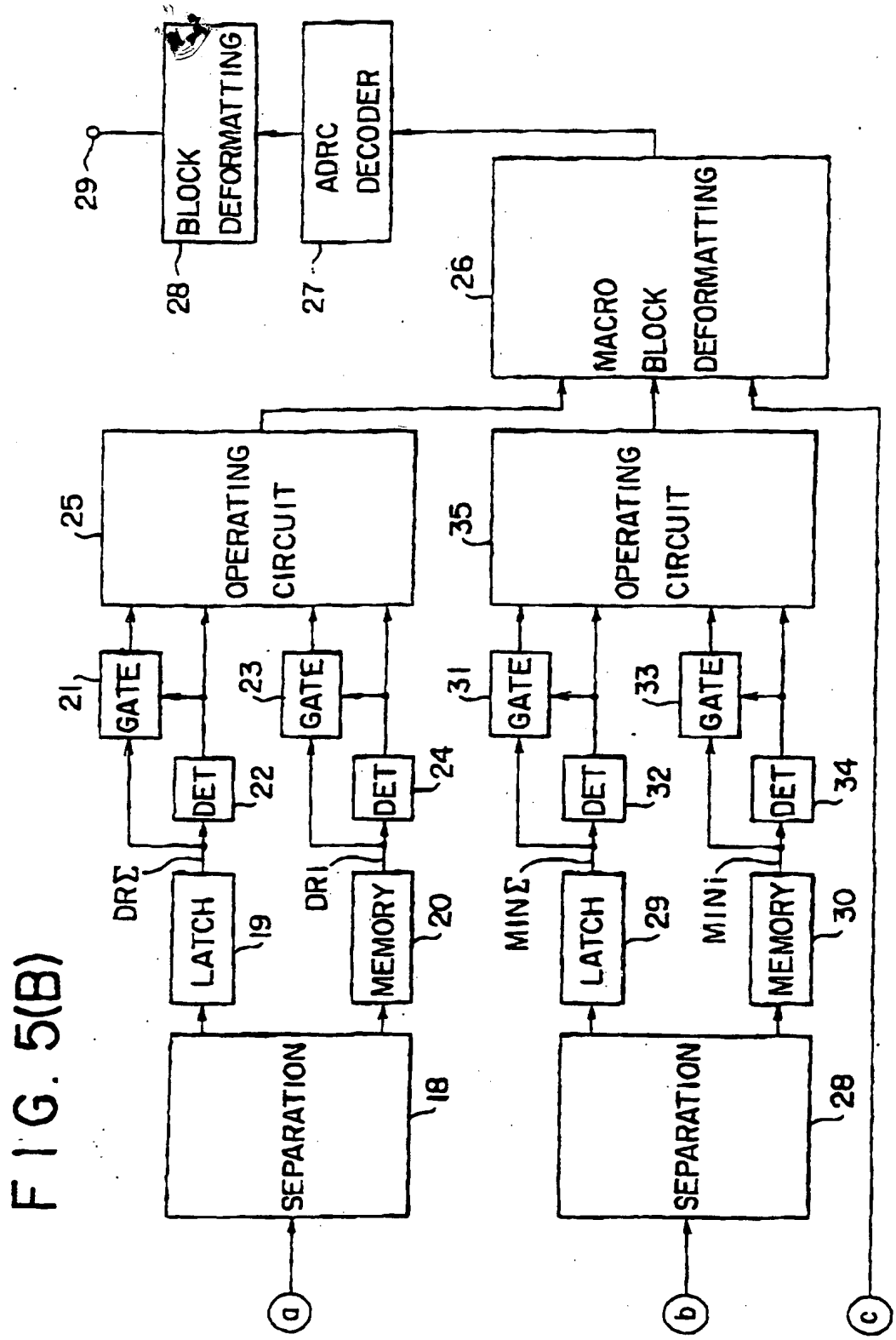

FIG. 5(B)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 6894

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y A	EP-A-0 318 244 (CANON K.K.) * column 5, line 3 - column 7, line 56 * ---	1-6 7-17	H04N7/13 H04N5/92 H04N5/926
Y	US-A-4 984 076 (WATANABE ET AL.) * column 3, line 7 - column 7, line 4 * ---	1-5	H04N7/26 H04N7/30 H04N7/54
Y	EP-A-0 430 631 (SONY CORPORATION) * column 4 - column 7, line 9 * -----	6	H04N7/64

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	26 October 1995	Materne, A

CATEGORY OF CITED DOCUMENTS

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